WHITE PAPER

PCI Express® Test Overview

KEYSIGHT

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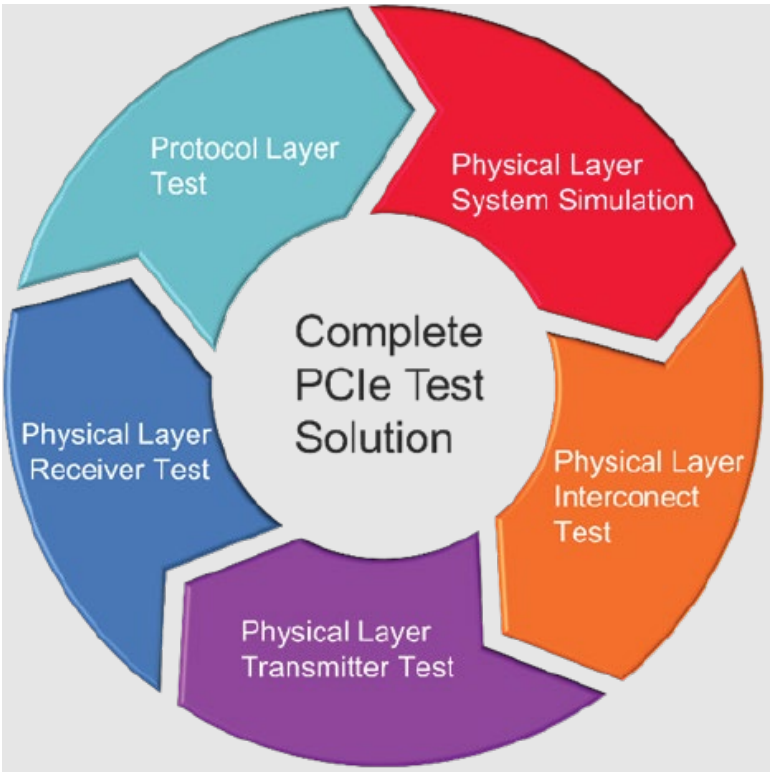
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Keysight's Complete and Scalable PCIe® Test Solutions from Simulation to Protocol





Introduction

PCI Express®, short for Peripheral Component Interconnect Express, is a high-performance and high-bandwidth serial communication interconnect standard. First proposed by Intel and further developed by the Peripheral Component Interconnect Special Interest Group (PCI-SIG) in replacement of bus-based communication architecture, such as PCI, PCI Extended (PCI-X), and Accelerated Graphics Port (AGP).

PCIe significantly improves system throughput, scalability, and flexibility at lower production cost, which is impossible to achieve all while using traditional bus-based interconnect. PCIe provides lower latency and higher data transfer rates than legacy parallel buses such as PCI and PCI-X. Every device that is connected to a motherboard with a PCIe link has its own dedicated point-to-point connection. This means that devices are not competing for bandwidth because they are not sharing the same bus.

Peripheral devices associated with PCIe technology for data transfer include graphics adapter cards, network interface cards (NICs), solid state drive (SSD) storage devices, storage accelerator devices, inference engines in artificial intelligence (AI) applications and other high-performance peripherals. With PCIe, data center managers can take advantage of high-speed networking across server backplanes, and connect to Gigabit Ethernet, Redundant Arrays of Independent Disks (RAID), and InfiniBand networking technologies outside of the server rack.

PCIe 5.0 brings 128 Gb/s of throughput, doubling the performance of PCIe 4.0. The specification is backwards compatible with all previous PCIe generations also offering new features, including electrical changes to improve signal integrity and backward-compatible card electromechanical (CEM) connectors for add-in cards.

PCIe 6.0 will double the bandwidth of PCIe 5.0 to 256 Gb/s among the same maximum number of lanes,16. The data transfer rate will hit 64 GT/s per pin, up from PCIe 5.0's 32 GT/s. A move from NRZ to PAM4 signals will bring new challenges. PCIe 6.0 is also backwards compatible with previous PCIe generations.

With solid industry-wide support and the dedication of PCI-SIG and various partner groups, PCIe has consistently demonstrated its ability to remain relevant, if not ahead of its time and, even performing, above and beyond other high-speed digital communication technologies.

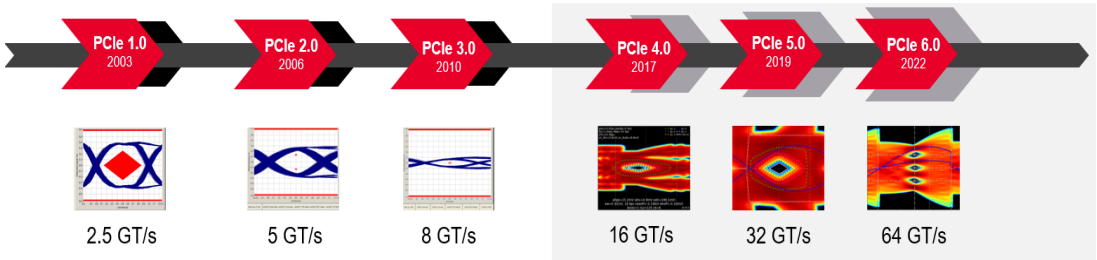


Figure 1. Development of the PCIe standard. PCIe 6.0 is moving to speeds up to 64 GT/s and PAM4 modulation.

Physical Layer – System Simulation

High-speed digital standards such as PCI Express 5.0 and 6.0 technologies are quickly evolving to keep pace with the data demand from emerging technologies such as 6G, the Internet of Things, artificial intelligence, virtual reality, and autonomous vehicles. Each generational change of high-speed computing standards provides new signaling features, faster data transfer rates, and smaller design margins. Faster speeds create new design challenges that require higher-accuracy simulation, new software tools, and more efficient workflows.

As a hardware engineer, your job is to design, verify, build, and test electronic products. If you fail to adopt new design methodologies, you risk product failure caused by degradation of high-speed signals in your printed circuit board (PCB). You also risk project delays, a skyrocketing budget, or jeopardizing your stellar reputation.

Avoiding this dilemma requires new design tools and a holistic design methodology that connects the workflows of multiple disciplines. With this approach, you can design for the myriad interface standards, without increasing design and verification time.

Keysight PathWave Advanced Design System (ADS) offers integrated design guidance via templates to help you get started faster with any PCIe generation design. Extensive component libraries make it easy to find the part you want. Automatic synchronization with layout allows you to visualize the physical layout while making schematic designs.

Pathwave ADS allows you to characterize and analyze the performance of your design early in the design cycle where errors can be quickly addressed before build-out, saving you both time and money and giving you more confidence in your end design. With Pathwave ADS you can simulate the effects of your channel on your PAM4 design while also applying your silicon-specific, adaptive equalization capabilities.

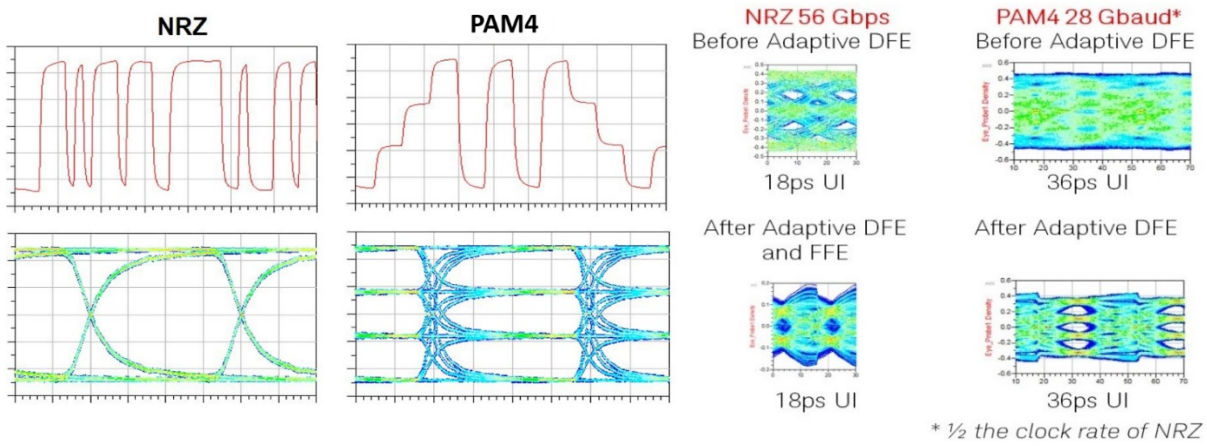


Figure 2. The ADS software allows you to simulate the effects of your specific channel including applied equalization here adaptive decision feedback equalization (DFE).

In addition, you can use the power of Pathwave ADS to simulate full channel effects of your PCIe 6.0 channel elements combined with your transmitter and receiver models.

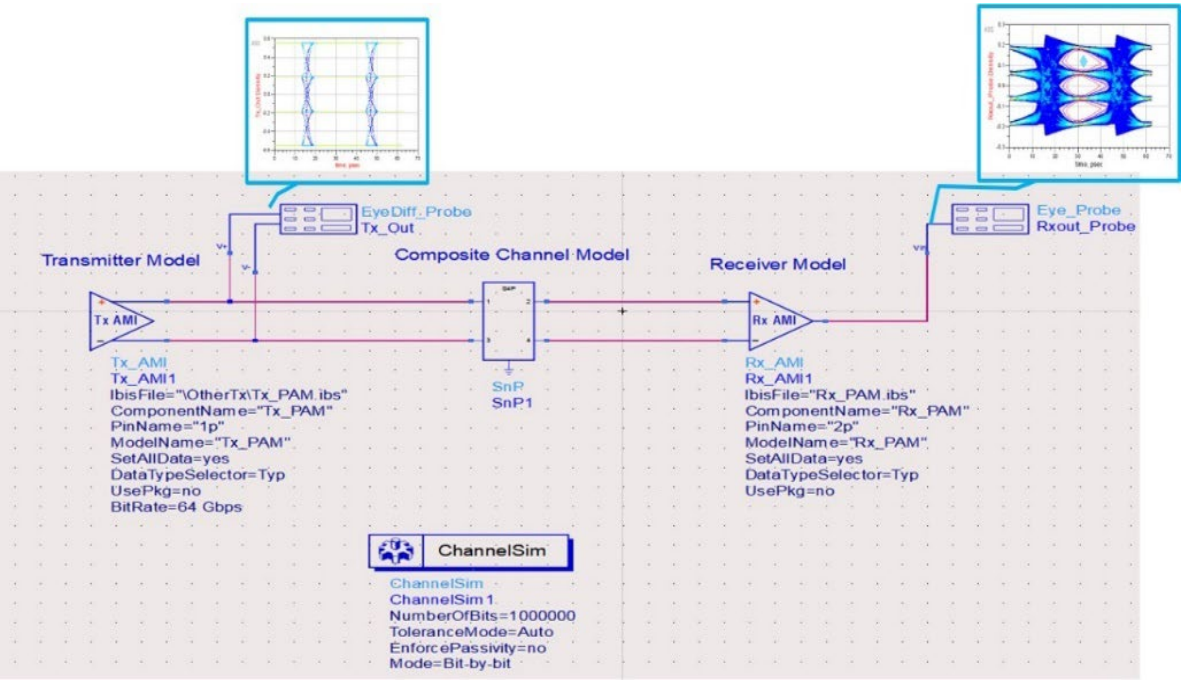


Figure 3. PCIe 6 system simulation with spec-based models

PathWave ADS has tools for all your pre-layout design exploration challenges. You can calculate line impedances with the Controlled Impedance Line Designer and model via behavior with the Via Designer. Optimizing link performance is possible with integrated circuit optimization. You can even understand where the signal is degraded with integrated time-domain reflectometry (TDR) analysis. With all these tools you will be able to minimize impedance mismatches and improve your margins.

Pathwave ADS will set you on the right path forward for your high-speed serial-link designs ensuring you can achieve the highest margins possible.

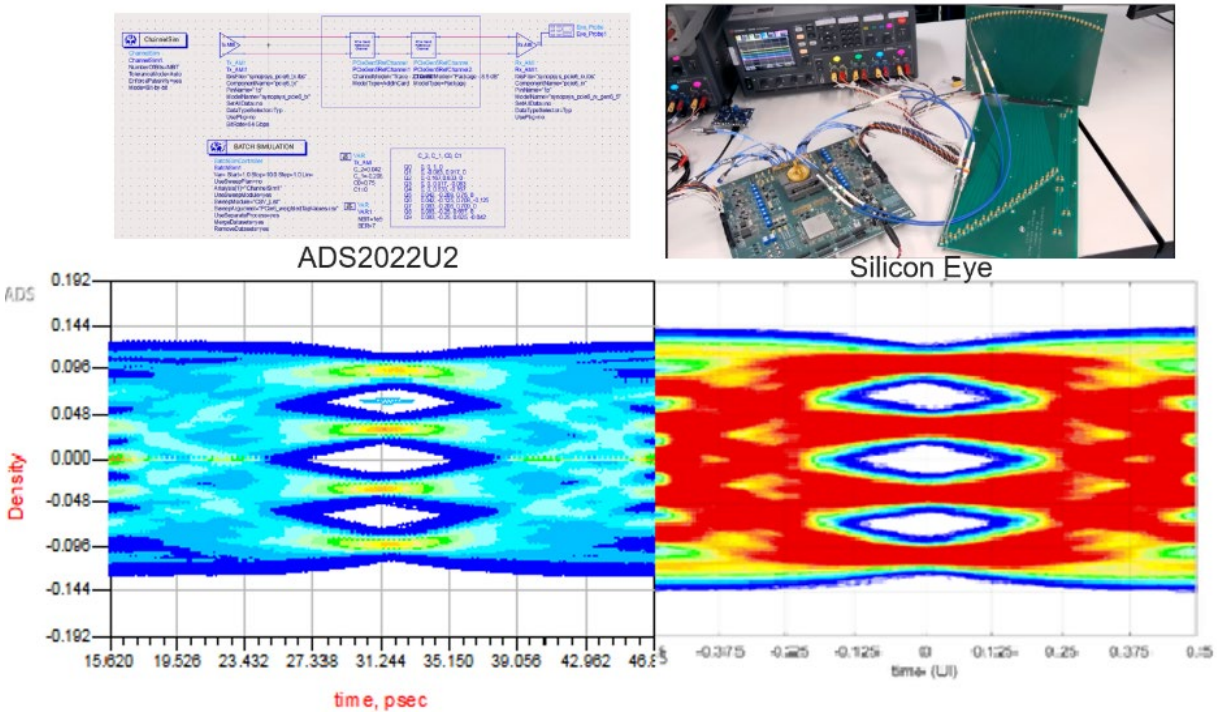


Figure 4. PCIe 6.0 simulation to measurement correlation

Get a quote for PathWave ADS bundles for PCIe simulation:

- W3625B PathWave ADS Core + EM Design + Layout + HSD Ckt Sim + SIPro + PIPro
- W3082E PathWave PCIe AMI Model Builder

Physical Layer – Interconnect Design

The previously simple channels of PCIe 4.0 and PCIe 5.0 have become more complex with the migration to PCIe 6.0 architecture due to a variety of performance-enhancing improvements. In many cases, PCIe 6.0 risers as shown in Figure 4 will need to be used for server applications to minimize the overall physical size constraints. This will create additional reflections, amplitude degradation and jitter problems. Comprehensive signal integrity analysis is now critical, including key measurements of crosstalk, PAM4 eye diagrams and insertion loss.

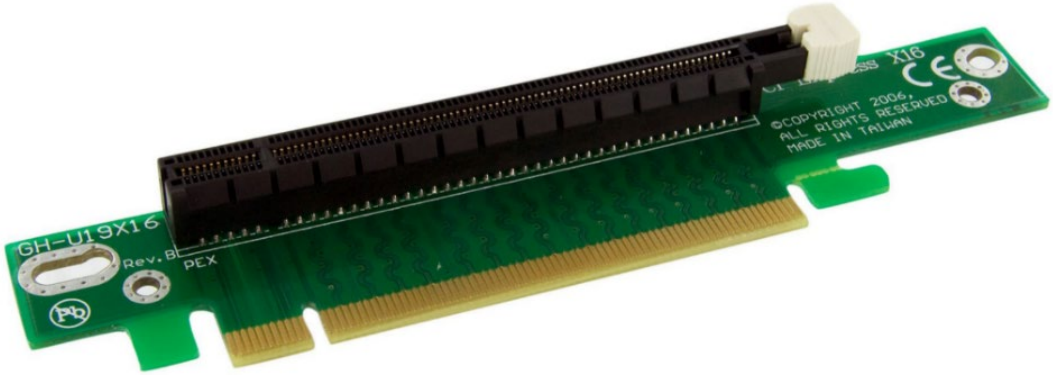


Figure 5. PCIe 6.0 riser creates additional signal integrity challenges

When designing the interconnects for PCI Express 6.0, you'll be facing new signal integrity challenges, especially in a few key areas:

Generating accurate PAM4 eye diagrams and quickly assessing the necessary equalization taps to open the eye. N19301 Physical Layer Test System (PLTS) software can do this quickly and easily with multi-channel simulation and automatic tap selection.

The adjacent channels of 64 Gbaud (128 Gbps) data transmission will cause more crosstalk than PCIe 5.0.

Characterization of the most susceptible channels within the PCIe 6.0 interconnect can be done with a 16-channel M937xA vector network analyzer and PLTS software.



Figure 6. The digital interconnect test system provides full signal integrity characterization of multiport interconnect products.

The PLTS software is a convenient tool to perform multi-domain characterization of PCIe 6.0 interconnect. Looking at a multi-domain analysis within the PLTS tool in Figure 7 shows a PCIe 6.0 riser stripline transmission line structure between two vias. We can create a standardized test template specific to the important performance parameters such as impedance profile (time-domain reflectometry), near-end crosstalk (NEXT) and far-end crosstalk (FEXT) in both time and frequency domain horizontal axes, mode conversion and PAM4 eye diagram. The eye diagram analysis is particularly helpful to gain insight because the design engineer can immediately see results of various stimulus/response scenarios. These PAM4 eye diagrams have 32 & 64 Gbaud (64 & 128 Gbps) data rates with 4 taps of decision feedback equalization (DFE). Color-grade histogram mode is utilized for the 32 Gbaud eye in the first case. This is accomplished through a multi-channel simulator built directly into the PLTS tool without forcing the user to create time consuming simulation schematics. This cuts development of PCIe 6.0 interconnect by a factor of 4 times and enables a much more efficient design cycle.

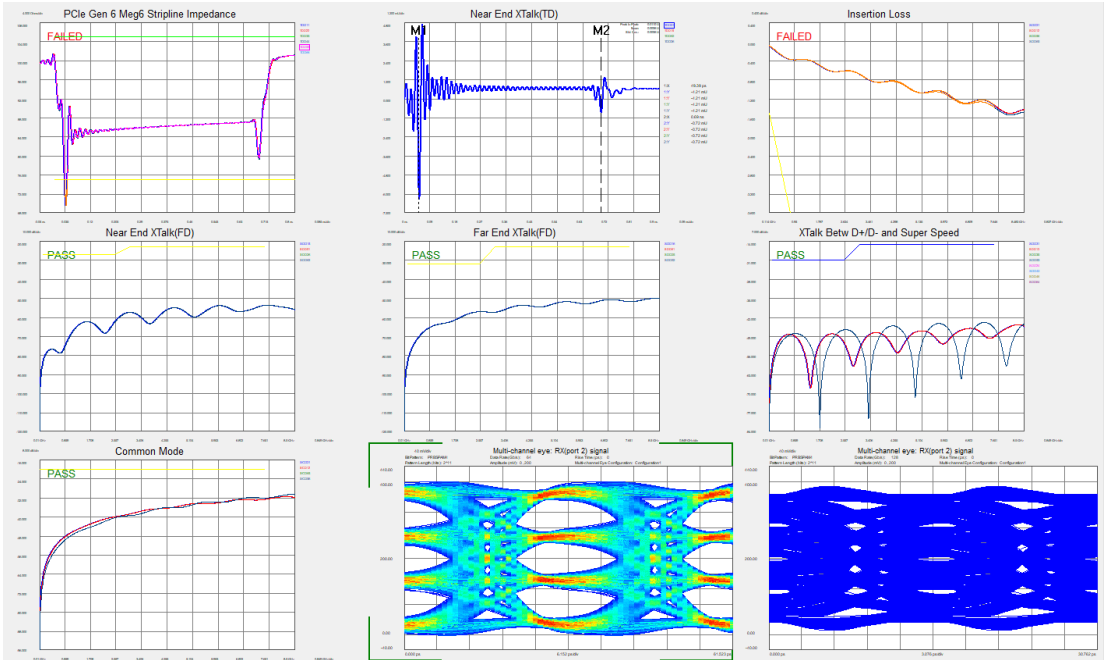


Figure 7. PCIe 6.0 stripline transmission line structure between two vias, characterized with the PLTS software

Get a quote for the digital interconnect test system reference solution

Physical Layer – Transmitter Test

The PCI Express 5.0 standard supports data rates up to 32 GT/s whereas the PCIe 6.0 specification doubles the data rate again to 64 GT/s utilizing PAM4 signaling technology while preserving the same channel bandwidth used by PCIe 5.0 devices. Both PCIe 5.0 and 6.0 technology represent closed-eye specifications. This means that the ability of the PCIe link to achieve its target throughput and performance is based upon a combination of transmitter and receiver equalization being applied to overcome the physical limitations of the transmitter channel including package and connector effects along with transmission line losses and reflections.

To help you characterize your transmitter at both the silicon level and at the system level, Keysight offers an automated transmitter test solution based on the class leading UXR family of oscilloscopes with bandwidths of up to 110 GHz.



Figure 8. Low-noise UXR real-time oscilloscopes with up to 110 GHz bandwidth for most accurate PCIe TX test

As PCI Express speeds increase, channel loss also has a greater impact on your device's signal-to-noise ratio (SNR). With PCIe 6.0 moving to PAM4 signal encoding, the impact to your measurements forces you to accommodate an additional decrease in SNR of 9 dB. The UXR series oscilloscopes have an intrinsic noise floor that is up to half of that of any other oscilloscope ever offered. This was done with standards like the PCI Express 6.0 specification in mind and the UXR is able to make the most accurate transmitter measurements compared to any other real-time oscilloscope.

Transmitter test automation

Keysight offers two automated transmitter compliance test tools for PCI Express along with other high-performance serial bus standards. The D9050PCIC PCI Express 5.0 electrical performance and compliance test software provides you with a fast and straightforward way to verify and debug your PCIe Express 5.0 design for both silicon validation (per the PCIe 5.0 BASE specification) as well as for PCIe 5.0 add-in cards and motherboard systems. Keysight also provides a separate transmitter test application covering testing of devices designed according to the PCIe 4.0 specification.

The D9040PCIC PCI Express electrical performance validation and compliance software covers the testing of devices designed according to the PCIe 3.0 or PCIe 4.0 specification.

The PCI Express D9050PCIC test software allows you to automatically execute PCI Express electrical transmitter tests, and it displays the results in a flexible report format. In addition to the measurement data, the report provides a margin analysis that shows how closely your device passed or failed each test.

The D9050PCIC PCI Express electrical performance validation and compliance software performs a wide range of electrical tests as per the PCI Express 5.0 specification only and supports testing transmitters that operate at 32, 16, 8, 5, and 2.5 GT/s. In addition to full swing (800 mV) testing, the software also supports testing for low-power, half-swing devices (400 mV).

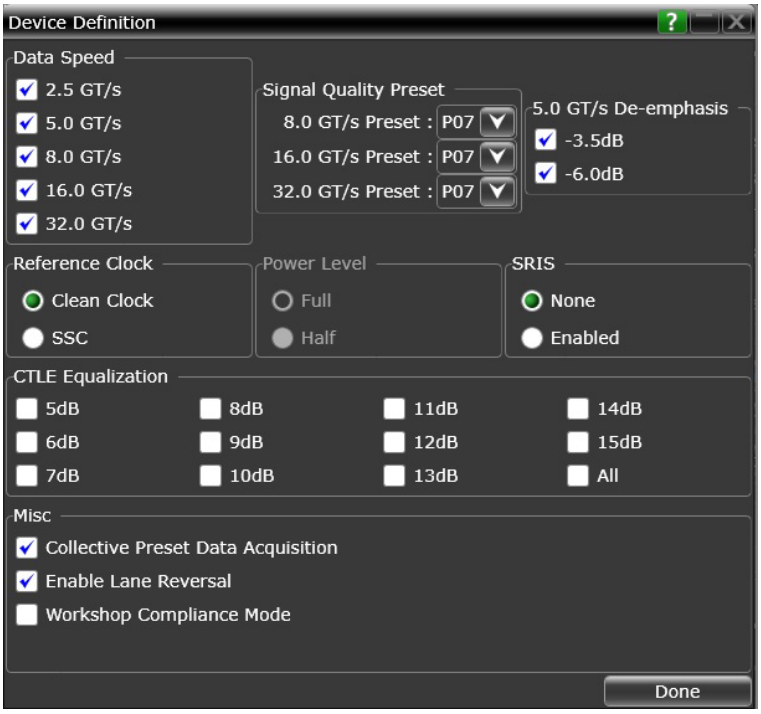


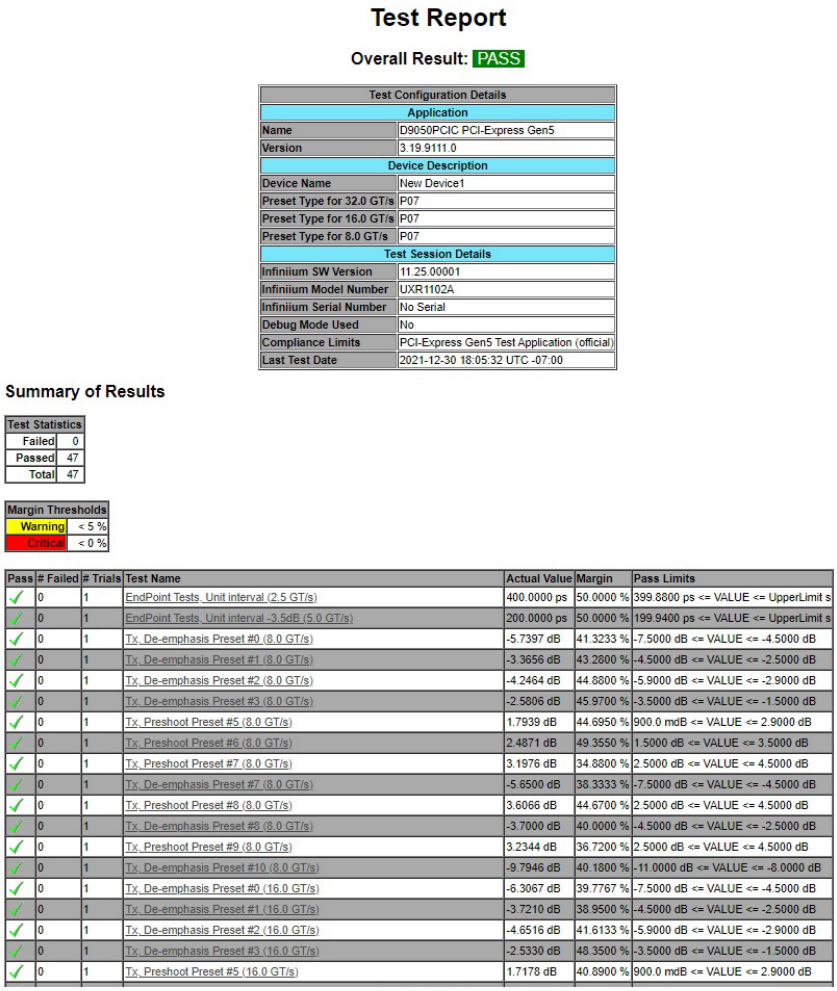
Figure 9. Save TX performance validation test time with the D9050PCIC PCIe test automation software

The D9050PCIC PCI Express electrical test software saves you time by setting the stage for automatic execution of PCI Express electrical tests. Part of the difficulty of performing electrical tests for PCI Express is hooking up the oscilloscope, loading the proper setup files, and then analyzing the measured results by comparing them to limits published in the specification. The PCI Express electrical test software does much of this work for you. In addition, if you discover a problem with your device, robust debug tools are available to aid in root-cause analysis.

The D9050PCIC software also has an integrated interface for controlling the InfiniiSim waveform transformation toolset for de-embedding of test fixtures and for easily adding the appropriate loss functions needed to complete CEM 5.0 testing at 32 GT/s.

Introduced with PCIe 2.0, de-embedding of test fixtures utilizes S-parameters as input to create a de-embed model that helps to restore high-frequency signal content that is often lost or significantly attenuated by test fixtures and cables. This can help to recover significant jitter margin normally lost to fixtures used in a test setup. This helps ensure consistent run-to-run setup of the instrumentation, saving you time and providing consistent and accurate receive test results. As an alternative to de-embedding using S-parameter files, the D9050PCIC also supports the use of selecting a PCIe 5.0 continuous-time linear equalization (CTLE) level to help compensate for break-out board losses.

When completed, the D9050PCIC app provides you with an HTML report summarizing the tests performed on your device.



Test Report

Overall Result: PASS

Test Configuration Details	
Application	
Name	D9050PCIC PCI-Express Gen5
Version	3.19.9111.0
Device Description	
Device Name	New Device1
Preset Type for 32.0 GT/s	P07
Preset Type for 16.0 GT/s	P07
Preset Type for 8.0 GT/s	P07
Test Session Details	
Infiniium SW Version	11.25.00001
Infiniium Model Number	UXR1102A
Infiniium Serial Number	No Serial
Debug Mode Used	No
Compliance Limits	PCI-Express Gen5 Test Application (official)
Last Test Date	2021-12-30 18:05:32 UTC -07:00

Summary of Results

Test Statistics	
Failed	0
Passed	47
Total	47

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	EndPoint Tests, Unit interval (2.5 GT/s)	400.0000 ps	50.0000 %	399.8800 ps <= VALUE <= UpperLimit s
✓	0	1	EndPoint Tests, Unit interval -3.5dB (5.0 GT/s)	200.0000 ps	50.0000 %	199.9400 ps <= VALUE <= UpperLimit s
✓	0	1	Tx, De-emphasis Preset #0 (8.0 GT/s)	-5.7397 dB	41.3233 %	-7.5000 dB <= VALUE <= -4.5000 dB
✓	0	1	Tx, De-emphasis Preset #1 (8.0 GT/s)	-3.3656 dB	43.2800 %	-4.5000 dB <= VALUE <= -2.5000 dB
✓	0	1	Tx, De-emphasis Preset #2 (8.0 GT/s)	-4.2464 dB	44.8800 %	-5.9000 dB <= VALUE <= -2.9000 dB
✓	0	1	Tx, De-emphasis Preset #3 (8.0 GT/s)	-2.5806 dB	45.9700 %	-3.5000 dB <= VALUE <= -1.5000 dB
✓	0	1	Tx, Preshoot Preset #5 (8.0 GT/s)	1.7939 dB	44.6950 %	900.0 mdB <= VALUE <= 2.9000 dB
✓	0	1	Tx, Preshoot Preset #6 (8.0 GT/s)	2.4871 dB	49.3550 %	1.5000 dB <= VALUE <= 3.5000 dB
✓	0	1	Tx, Preshoot Preset #7 (8.0 GT/s)	3.1976 dB	34.8800 %	2.5000 dB <= VALUE <= 4.5000 dB
✓	0	1	Tx, De-emphasis Preset #7 (8.0 GT/s)	-5.6500 dB	38.3333 %	-7.5000 dB <= VALUE <= -4.5000 dB
✓	0	1	Tx, Preshoot Preset #8 (8.0 GT/s)	3.6066 dB	44.6700 %	2.5000 dB <= VALUE <= 4.5000 dB
✓	0	1	Tx, De-emphasis Preset #8 (8.0 GT/s)	-3.7000 dB	40.0000 %	-4.5000 dB <= VALUE <= -2.5000 dB
✓	0	1	Tx, Preshoot Preset #9 (8.0 GT/s)	3.2344 dB	36.7200 %	2.5000 dB <= VALUE <= 4.5000 dB
✓	0	1	Tx, De-emphasis Preset #10 (8.0 GT/s)	-9.7946 dB	40.1800 %	-11.0000 dB <= VALUE <= -8.0000 dB
✓	0	1	Tx, De-emphasis Preset #0 (16.0 GT/s)	-6.3067 dB	39.7767 %	-7.5000 dB <= VALUE <= -4.5000 dB
✓	0	1	Tx, De-emphasis Preset #1 (16.0 GT/s)	-3.7210 dB	38.9500 %	-4.5000 dB <= VALUE <= -2.5000 dB
✓	0	1	Tx, De-emphasis Preset #2 (16.0 GT/s)	-4.6516 dB	41.6133 %	-5.9000 dB <= VALUE <= -2.9000 dB
✓	0	1	Tx, De-emphasis Preset #3 (16.0 GT/s)	-2.5330 dB	48.3500 %	-3.5000 dB <= VALUE <= -1.5000 dB
✓	0	1	Tx, Preshoot Preset #5 (16.0 GT/s)	1.7178 dB	40.8900 %	900.0 mdB <= VALUE <= 2.9000 dB

Figure 10. Test report in D9050PCIC PCIe test automation software

With the SW00PCIE PCI Express validation license suite you get the above PCIe TX test automation license covering the PCI Express technology generations starting from PCIe 4.0. Together with the subscription model, you will get PCIe 6.0 automation as soon as it becomes available. The same applies to the SW02PCIE license suite which additionally offers PCIe protocol decoding/triggering. For PAM4-modulated signals starting at Gen 6, the D9020PAMA pulse amplitude modulation PAM-N analysis software enables you to characterize PAM4 and higher modulation electrical signals accurately and quickly. These options are required for all PCIe 6.0 compliance testing.

Get a quote on a PCIe 5.0 transmitter compliance test solution or a PCIe 6.0 transmitter compliance test solution

Physical Layer – Receiver and Link Equalization Test

With 8 GT/s, starting with PCI Express 3.0 upwards, the PCI Express standard introduced an active transmit equalization adaptation during link bring up. This allows the receiver to not only change its equalization to the channel conditions but also the equalization of its link partner's transmitter. This equalization negotiation allows devices, designed according to the PCI Express 3.0 and above revisions, to maximize the allowable channel reach as well as tuning performance to match a channel's analog characteristics which are unknown to the link partners until the link training is asserted. Active link training is one of the features of the PCI Express standard which enables the combination of any PCI Express compliant mainboard to work with any PCI Express compliant add-in card.

The classical receiver test, using non-protocol-aware test equipment, can test the receiver's ability to deal with the stress signal if the correct transmitter equalization is determined by trial and error for example. But it would not be able to test the device's ability to negotiate a working transmit equalization with its link partner which would be the receiver tester's pattern generator. Thus, new tests and new abilities in the receiver testers were required. The new tests are referred to as the *Link Equalization Tests.*

Link Equalization Receiver Tests check the DUT's ability to negotiate a transmit equalization with its link partner as well as its receiver's equalization adaptation capabilities for a worst-case stress signal. Like in the classical receiver test, the proper functioning is confirmed by measuring the bit error ratio after the link was brought into loopback. Stress signal calibration is complex and time consuming. It requires a real-time oscilloscope with a bandwidth fitting to the rise time of the stress signal generator, the pattern generator of the receiver test system. Test automation is highly recommended. Since PCI Express 4.0, the classical receiver test for 8 GT/s and higher transfer rates has been replaced by the *Link Equalization Receiver Test in the PCI Express Architecture PHY Test Specification.*

Link Equalization Transmitter Tests check the DUT's ability to execute on the transmit equalization change requests sent by the link partner, the receiver tester in this case. Endpoint devices are tested for this during phase 1 as well as during phase 3, while root complex devices are tested during phase 2 of the link equalization phases of the target transfer rate. The test focuses on the electrical execution of the request as well as on the response time to the request during phase 2 and phase 3. A real-time oscilloscope is required for the equalization measurement as well as for the response time measurement. For the response time measurement, the real-time oscilloscope needs to capture the signal from the receiver tester pattern generator as well as from the DUT transmitter. The signals are differential. Thus, either a four-channel oscilloscope or a two-channel oscilloscope with differential probes is required. Differential probes offering sufficient bandwidth for 8 GT/s and 16 GT/s are available.

Receiver and link equalization testing for PCI Express 5.0 and 6.0

The M8040A 64 Gbaud high-performance BERT is approved for *LinkEQ Gold Suite* testing for 8 GT/s and 16 GT/s and is used at PCI-SIG workshops covering 32 GT/s. It was also used for pathfinding for PCIe 6.0 64 GT/s. Until the time of publishing of this solution overview, PCIe 6.0 testing has not made it into the PCI Express Architecture PHY Test specification. The perfect oscilloscope for a M8040A-based PCIe RX and LinkEQ test bench is a UXR0594A Infiniium UXR-Series oscilloscope. The very good intrinsic noise performance of the UXR-Series and the M8040A's coverage of baud rates beyond 32 Gbaud combined with its NRZ and PAM4 coding capabilities make this combination the ideal choice for users with PCIe 6.0 testing needs on the horizon. An alternative oscilloscope for PCIe 5.0 (but not for PCIe 6.0) is the DSAZ592A Infiniium Z-Series oscilloscope with 59 GHz (two channels) and the DSAZ334A Infiniium Z-Series oscilloscope with 33 GHz (four channels).

Test automation software is available for PCIe 5.0 Base specification (N5991PB5A) and CEM form factor (N5991PC5A), as well as for PCIe 6.0 for Base specification (N5991PB6A).

The J-BERT M8020A-based setup can be used for PCIe 5.0 & PCIe 6.0 RX and LinkEQ testing up to and including 16 GT/s. But it is not supported by the PCIe 6.0 test automation software.

Table 1. Keysight PCIe 5.0 and 6.0 receiver test automation solutions

PCIe 5.0 RX Test Automation	PCIe 6.0 RX Test Automation
N5991PB5A for Base spec with M8020A (up to16 GT/s) or M8040A	N5991PB6A for Base spec with M8040A
5991PC5A for CEM spec with M8020A (up to16 GT/s) or M8040A	
Get a quote on the PCIe 5.0 receiver compliance test solution	Get a quote on PCIe 6.0 receiver test solution

Receiver and link equalization testing for PCI Express 4.0

A maximum transfer rate of 16 GT/s and all NRZ signaling, PCI Express 4.0 receiver and link equalization testing can be well addressed with the J-BERT M8020 high-performance BERT system. A UXR0334A Infiniium UXR-Series oscilloscope with 33 GHz bandwidth and four channels, it makes for an excellent choice together with the J-BERT M8020A high-performance BERT system. Alternative real-time oscilloscopes can be the DSAZ334A Infiniium Z-Series oscilloscope with 33 GHz and four channels or the DSAV334A Infiniium V-Series oscilloscope with 33 GHz and four channels. In the case of the V-Series oscilloscope, a differential probing system with at least 25 GHz of bandwidth for the link equalization response time tests would be recommended. The minimum acceptable bandwidth for the real-time oscilloscope in combination with a J-BERT M8020A would be 25 GHz. The J-BERT M8020A high-performance BERT system is approved for LinkEQ Gold Suite testing of 8 GT/s and 16 GT/s at PCI-SIG compliance workshops.

The M8040A 64 Gbaud high-performance BERT is approved for LinkEQ Gold Suite testing for 8 GT/s and 16 GT/s also. The ideal oscilloscope for a M8040A-based PCIe Rx and LinkEQ test bench would be a UXR0594A Infiniium UXR-Series. The unmatched intrinsic noise performance of the UXR Series and the M8040A's coverage of baud rates beyond 32 Gbaud combined with its NRZ- and PAM4-coding capabilities make this combination the ideal choice for users with PCIe 5.0 and PCIe 6.0 testing needs on the horizon. Alternative oscilloscopes are the DASZ592A Infiniium Z-Series oscilloscope with 59 GHz (two channels) and the DSAZ334A Z-Series oscilloscope with 33 GHz (four channels). The Z-Series oscilloscopes are supported for PCIe 5.0 but not for PCIe 6.0. The minimum bandwidth for an oscilloscope for a M8040A-based setup not using transition time converters is 50 GHz.

Test automation software is available for PCIe 4.0 for Base specification (N5991PB4A), CEM form factor (N5991PC4A), M.2 form factor (N5991PM4A), and the U.2 form factor (N5991PU4A). N5991PM4A and N5991PU4A currently support 8 GT/s testing only.



Figure 11. M8040A 64 Gbaud high-performance BERT

Designed for NRZ and PAM4 receiver testing with baud rates exceeding 32 Gbaud, the M8040A 64 Gbaud high-performance BERT is Keysight's answer for PCI Express receiver and LinkEQ testing needs for transfer rates from 2.5 GT/s to 64 GT/s.

The M8040A system capabilities can be extended when the need arises. The pattern generator and error detector starting configurations are for NRZ and 32 Gbaud. PAM4 capabilities can be upgraded.

Stress conditions are achieved by the inter-symbol interference (ISI) via traces which are part of the PCI Express fixture kits. Option M8045A-0G3 activates required jitter sources and the M8054A interference module or the M8194A/95A/96A arbitrary waveform generator (AWG) modules can be used as interference sources.

The M8045A pattern generator can use a DUT's 100 MHz reference clock for its clock generation. Option M8045A-0G6 provides the necessary reference clock multiplier with sufficient bandwidth to transfer spread-spectrum clocking (SSC).

A five-tap de-emphasis is added with option M8045A-0G4. The M8057B remote head is recommended for PCIe RX and LinkEQ testing. The de-emphasis option together with the PCIe skip ordered set (SKP OS) filtering options enable the use of the PCIe TX equalization (TxEQ) coefficient matrix on the pattern generator. The TxEQ matrix can be generated for any number of filler symbols (FSs) between 24 and 63. This is useful to check if the DUT can handle link partners advertising different FS values.

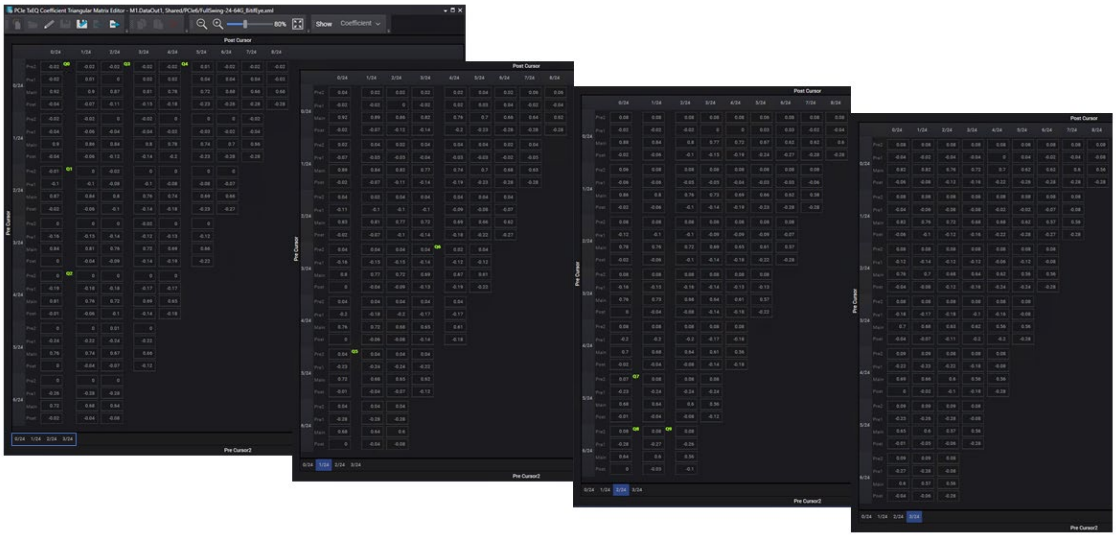


Figure 12. Example for PCIe 6.0 64 GT/s TxEQ matrix for 24 FSs. For each Pre-cursor2 value, a matrix for Precursor1 and Postcursor is displayed. The actual M8045A coefficient settings, which will be applied when a call is made, can be edited. This allows individual calibration of each cell.

The system offers a Link Training and Status State Machine (LTSSM), which can train DUTs, into loopback through L0 / recovery on any lane which can act as a logical lane 0, or through configuration on any lane. The LTSSM, M8046A-0S1, covers 8 GT/s, 16 GT/s, 32 GT/s and with the LTSSM extension option M8046A-0N1 even 64 GT/s. Starting with 32 GT/s, the LTSSM can use speed bypass for DUTs supporting this mode. An alternative is training through configuration with equalization which enables LinkEQ testing on lanes which cannot act as a logical lane 0.

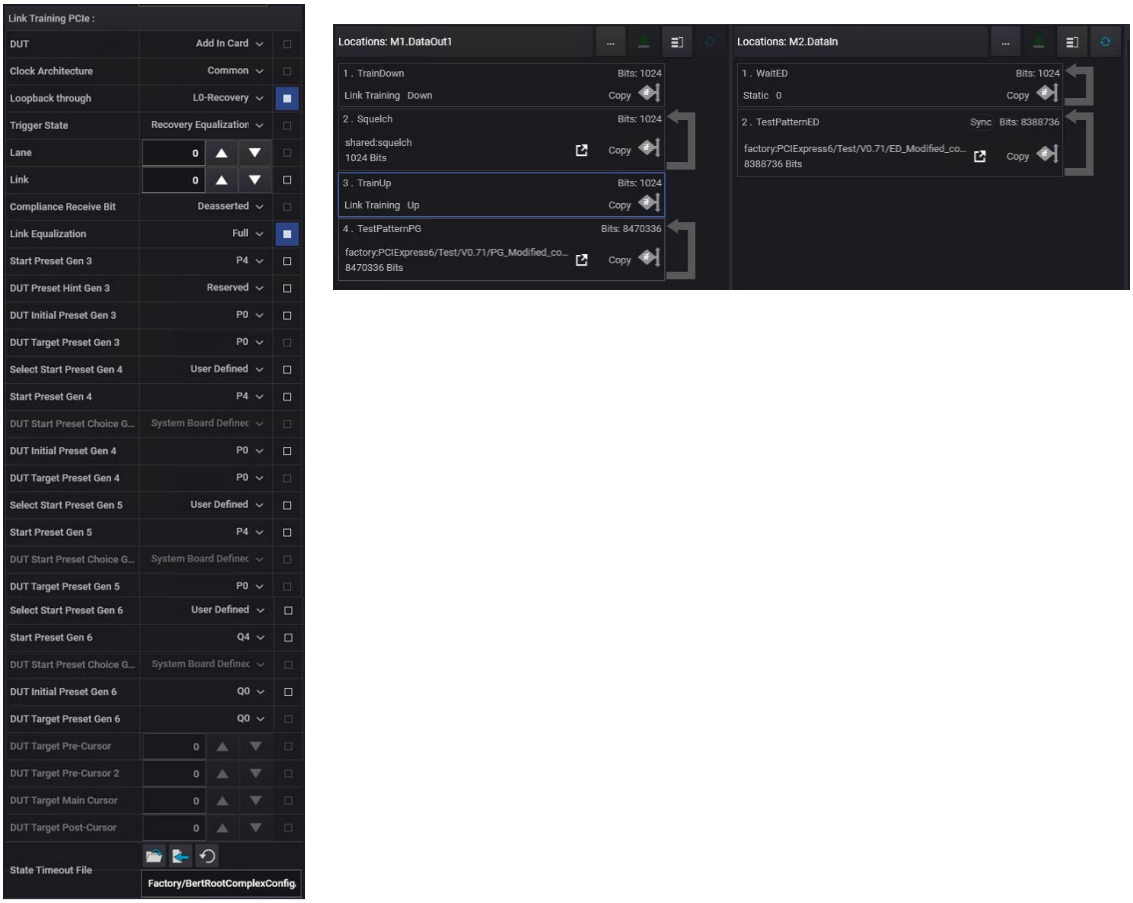


Figure 13. View of the link training setup

The error detector of the M8040A system, the M8046A, can be equipped with a clock data recovery (CDR), option -0A4, and with SKP OS filters for transfer rates up to and including 32 GT/s, option -0S2, as well as 64 GT/s with the extension option -0N2.

Backchannels, the channels between the DUT transmitter and the error detector, will in most cases require equalization capabilities. The M8046A error detector is equipped with a 16-tap feed-forward equalization (FFE). Additionally, the M8047 re-driver series will add CTLE-based equalization. The use of the M8047 redriver series is recommended for system test of 8 GT/s and higher as well as for add-in card (AIC) testing of 16 GT/s and higher.

The J-BERT M8020A was specifically designed for PCIe RX and LinkEQ testing up to and including 16 GT/s with option M8041A/51A-C16. It offers the highest level of integration of the M8000 BERT series.

All impairments are built-in, including interference options -0G3 and -0G7, error detector clock recovery and equalization option -0A3, and pattern generator de-emphasis option -0G4.



Figure 14. J-BERT M8020A high-performance BERT offers highest integration.

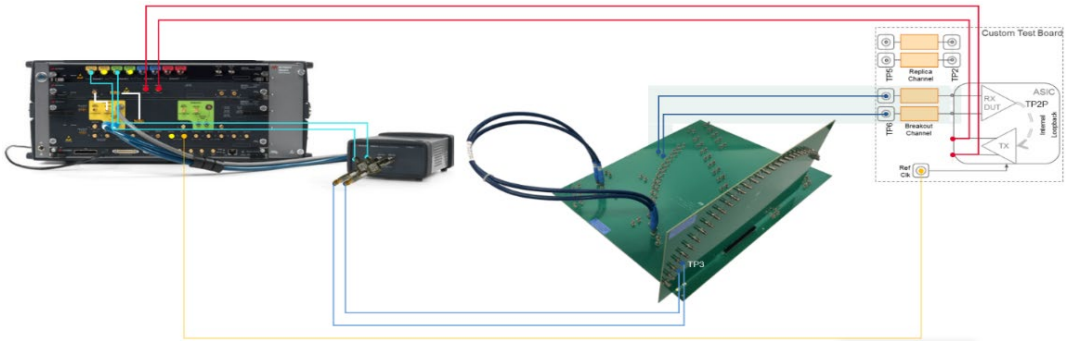
The system can be equipped with four data channels when the main BERT module M8041A is accompanied by the data channel expander module M8051A. A PCIe LTSSM is available for the data channel 1 of each module which can test any lane that can act as a logical lane 0.
The LTSSM is option -0S4. The error detectors will filter PCIe SKP OS with option -0S2.

PCI Express RX and LinkEQ test automation

The N5991 PCI Express RX and LinkEQ test automation family is designed to meet the needs of the data center application space, with many high-speed links within and between servers. It utilizes the Keysight M8000 high-performance BERT Series as well as Keysight's real-time oscilloscopes.

Starting with PCI Express 3.0, the receiver stress signal calibration targets are defined as eye height and eye width after applying a reference receiver, which adapts to the stress signal. The concept of transmitter de-emphasis optimization also needs to be considered. This requires special tools to determine the eye height and eye width. For Base specification calibrations, the preferred method is SEASIM (statistical eye analysis simulation), which simulates the stress signal and reference receiver using a step measurement through the setup to determine channel characteristics and impairment parameters.

In contrast, stress signal calibrations following the PCI Express Architecture PHY test specification require the use of the waveform post-processing tool SIGTEST. In both cases, multiple eye-height and eye-width measurements must be averaged to achieve usable results per impairment and launch-amplitude, de-emphasis, and pre-shoot combinations. This requires many measurements and lengthy processing.



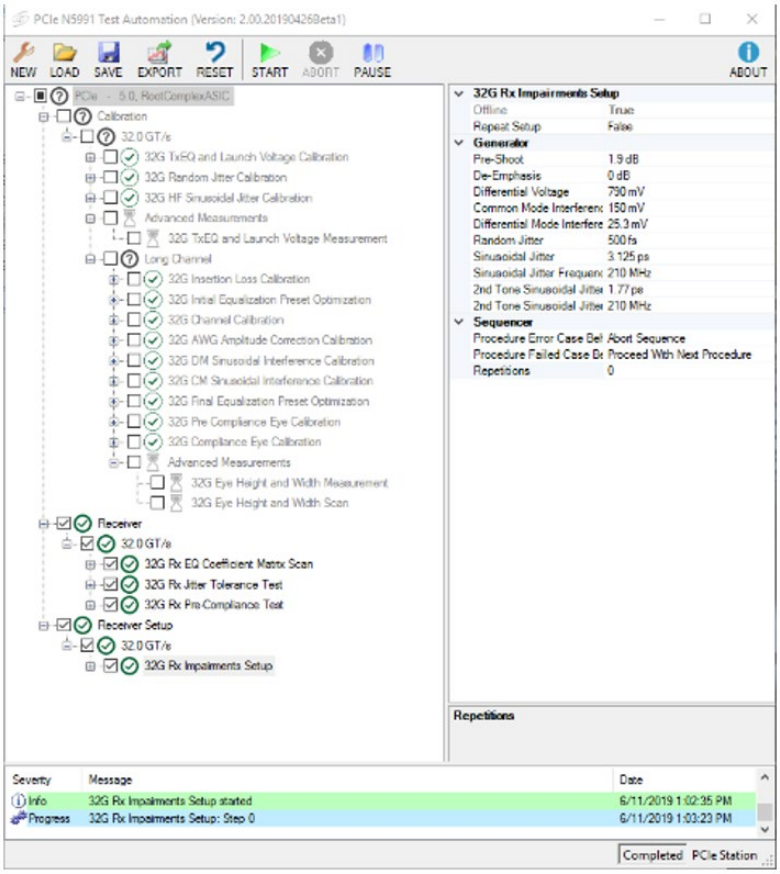


Figure 15. PCI Express calibration and receiver testing

Actual stress signal calibration procedures differ for 8 GT/s, 16 GT/s and 32 GT/s. For instance, PCI Express 3.0 8 GT/s uses random jitter and differential mode sinusoidal interference as the main adjustments to achieve target eye height and eye width, while for actual stress signal calibration, PCI Express 5.0 32 GT/s uses channel loss adjustment for a first eye height and eye width adjustment, followed by a tuning process using differential mode sinusoidal interference, sinusoidal jitter and launch amplitude. PCI Express 5.0 32 GT/s is like PCI Express 4.0 16 GT/s with a slightly modified stress signal calibration. Up to 32 GT/s, the stressed eye is defined for a bit error rate of 1e-12. PCI Express 6.0 64 GT/s uses PAM4 signaling. New measurements for pulse width jitter (PWJ) as well as signal-to-noise and distortion ratio (SNDR) are required for a 64 GT/s stressed-eye calibration. The stressed eye for 64 GT/s is defined for a first bit error rate of 1e-6.

The test procedure for 8 GT/s receivers, as defined in the PCI Express 3.0 Base specification, consists of stressed voltage tests for three different channel scenarios and one stressed jitter test. The PCI Express Architecture PHY test specification defines one combined test and, starting with PCI Express 4.0, the Base specification uses one combined receiver test too. Receiver testing for 16 GT/s common clock architecture (CC) in the PCI Express 4.0 Base specification uses residual SSC (rSSC) of 500 ps, while 16 GT/s for CC in the PCI Express 5.0 Base specification uses a 33 kHz sinusoidal jitter (SJ) spur of 1 ns.

Automation software for the calibration and test process, as well as a high-power PC, are highly recommended.

PCI Express link equalization testing

Link equalization is critical for PCI Express 8 GT/s, 16 GT/s and 32 GT/s because increases in data rates and server interconnect transmission path lengths create challenges for signal integrity. Signal equalizers at one or more locations in the link compensate for signal anomalies by boosting the high-frequency components. Link equalization testing verifies the optimization of the link between a transmitter and a receiver. The test solution acts as a link partner and quickly negotiates transmitter to receiver communications using protocol handshakes.

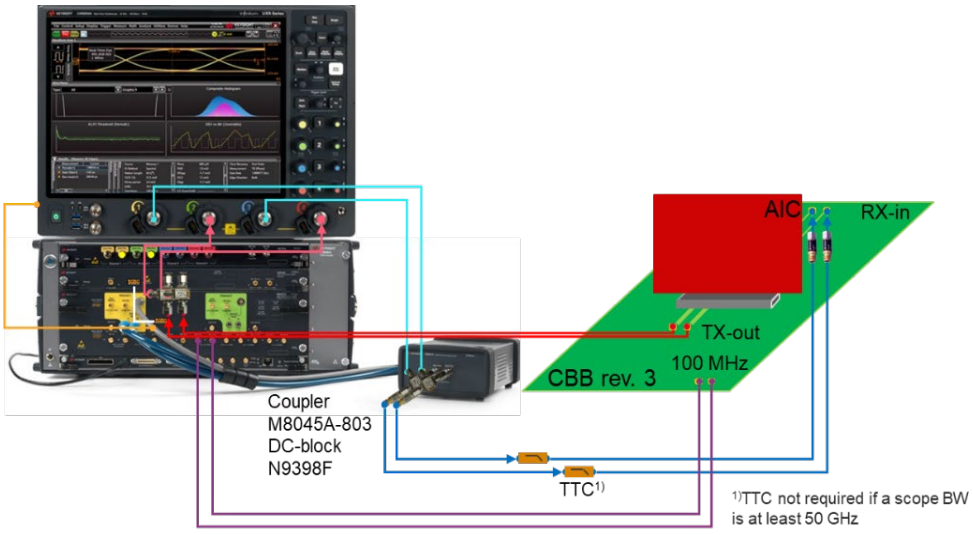


Figure 16. PCIe link equalization setup

Especially the link equalization response time test would be extremely time consuming to perform manually. The test automation controls all the instruments, starts the setup for each individual test and automatically analyzes the results. This includes protocol decoding of the waveforms as well as submitting the waveforms to SIGTEST for analysis of the applied preshoot and de-emphasis and changing the LTSSM for each preset and coefficient set to be measured.

Custom procedures

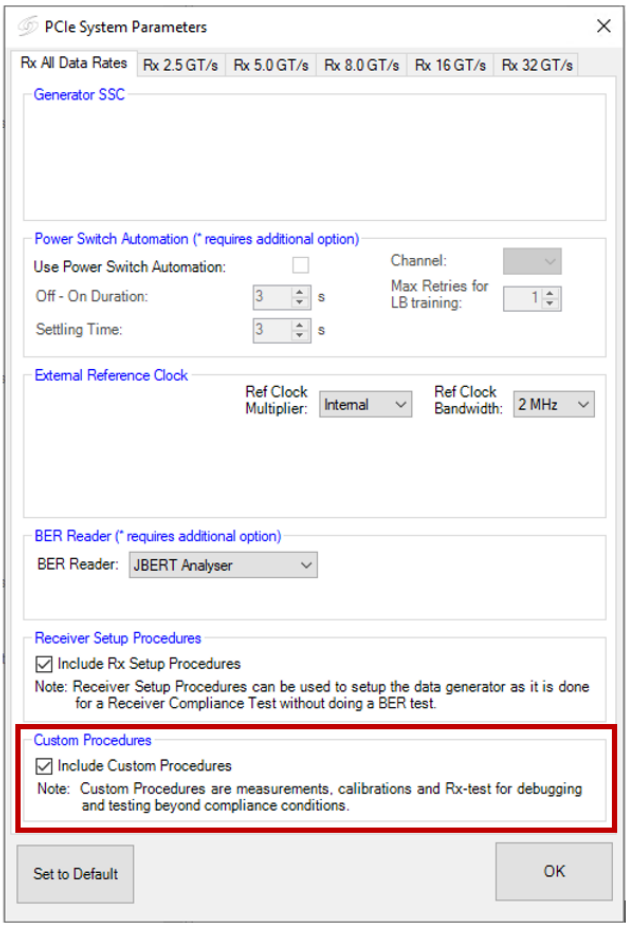


Figure 17. Custom calibrations are deactivated per default

All N5991P PCI Express receiver test automation products offer custom routines – additional measurements, calibrations and tests based on the calibration data. These routines provide further insight into the calibration data. To activate the custom routines, the Include Custom Procedure checkbox in the PCIe System Parameters window must be marked.

The TxEQ and Launch Voltage Measurement performs preshoot / de-emphasis as well as launch voltage measurements for user-provided target values. The measurement reports not only the target values and measured values but also the instrument-set values. This is very helpful to create TxEQ and launch voltage lookup tables for use in own test routines. The *TxEQ and Launch Voltage Measurement* is offered for 8 GT/s, 16 GT/s, 32 GT/s and 64 GT/s depending on the transfer rate coverage of the used product.

The *Eye Height and Width Measurement* performs eye measurements for user-provided impairment-, TxEQ- and launch voltage as well as reference receiver equalization parameters. The *Eye Height and Width Scan* offers multiple loop levels over relevant user-provided parameter ranges for eye measurements. Both custom measurements are available for 16 GT/s, 32 GT/s and 64 GT/s depending on transfer rate coverage of the used product. The same applies to the availability of custom calibrations.

Custom Eye Calibration (for 16 GT/s and 32 GT/s, depending on the transfer rate coverage of the used product) is like the *Compliance Eye Calibration* routine. But it logs found impairment combinations which lead to a compliant eye and not only the one that is closest to eye-height and -width targets. The *Custom Eye Scan Calibration* and the *Eye Height and Width Scan* enable a brute-force search of impairment combinations leading to compliant eyes.

The *Custom Tests* section allows performing RX compliance, jitter tolerance (JTOL) and sensitivity testing for the different impairment sets determined via the *Custom Calibration* procedures.

PCI Express base specification receiver tests

N5991PB6A is the newest addition to the N5991P PCI Express receiver test automation product family. It calibrates a stress signal and tests a device according to PCI Express Base specification 6.0. N5991PB4A and N5991PB5A implement receiver stress signal calibrations and tests according to PCI Express Base specification 4.0 and 5.0 respectively. Link equalization receiver and transmitter testing can be added with the N5991PA3A-ADD PCI Express Link EQ test support add-on. Link EQ testing at 32 GT/s is possible with the M8040A. There are no Link Equalization tests for 5 GT/s and 2.5 GT/s. Other add-ons are available for multi-channel support, DUT built-in error counter support and switch matrix support. Link EQ testing for 64 GT/s is planned for a later release and not available yet.

Table 2. PCIe Base spec test options for different transfer rates

Transfer rate	N5991PB6A	N5991PB5A	N5991PB4A
64 GT/S	M8040A	n/a	n/a
32 GT/s	M8040A, planned for a later release	M8040A	n/a
16 GT/s	M8040A, planned for a later release	M8040A or M8020A -16G [1]	M8040A, or M8020A 16G[1]
8 GT/s	M8040A, planned for a later release	M8040A or M8020A -16G/-8G [1]	M8040A, or M8020A 16G/8G [1]
5 GT/s	M8040A, planned for a later release	M8040A or M8020A -16G/-8G [1]	M8040A, or M8020A 16G/8G [1]
2.5 GT/s	M8040A, planned for a later release	M8040A or M8020A -16G/-8G [1]	M8040A, or M8020A 16G/8G [1]

1. M8020A-16G is an M8041A module with option -C16
M8020A-8G is an M8041A module with option -C08

PCI Express CEM specification receiver tests

N5991PC5A performs receiver stress signal calibrations and tests for 32 GT/s, 16 GT/s and 8 GT/s according to PCI Express Architecture PHY test specification 5.0. Stress signal calibration and tests for 5 GT/s as well as 2.5 GT/s are implemented according to PCI Express CEM specification 5.0. Changes to the calibration and test routines are possible since PCI Express Architecture PHY test specification 5.0 has not been released as of July 2022. Future releases will follow those changes; you can get new releases at no additional cost if you have a valid software maintenance license.

N5991PC4A implements receiver stress signal calibrations and tests for 16 GT/s and 8 GT/s according to PCI Express Architecture PHY test specifications 4.0 and 5 GT/s, as well as 2.5 GT/s receiver stress signal calibrations and tests are implemented according to PCI Express CEM specification 4.0.

Link equalization receiver and transmitter testing can be added with the N5991PA3A-ADD PCI Express LinkEQ test support add-on. LinkEQ testing at 32 GT/s is possible with the M8040A. There are no LinkEQ tests for 5 GT/s and 2.5 GT/s. Other add-ons are available for multi-channel support, DUT built-in error counter support and switch matrix support.

Table 3. PCIe CEM spec test options for different transfer rates

Transfer rate	N5991PC5A	N5991PC4A
32 GT/s	M8040A	n/a
16 GT/s	M8040A or M8020A -16G [1]	M8040A, or M8020A -16G [1]
8 GT/s	M8040A or M8020A -16G/-8G [1]	M8040A, or M8020A -16G/-8G [1]
5 GT/s	M8040A or M8020A -16G/-8G [1]	M8040A, or M8020A -16G/-8G [1]
2.5 GT/s	M8040A or M80200 -16G/-8G [1]	M8040A, or M8020A -16G/-8G [1]

1. M8020A-16G is an M8041A module with option -C16
M8020A-8G is an M8041A module with option -C08

PCI Express U.2 & M.2 specification receiver tests

So far compliance testing is defined for 8 GT/s only. Therefore, N5991PU4A PCIe 4.0 U.2 and N5991PM4A PCIe 4.0 M.2 RX test automation SW offer testing at 8 GT/s only. 16 GT/s testing will be added once 16 GT/s testing becomes part of the PCI Express compliance workshop testing. Valid software maintenance coverage will be required to use future N5991PU4A and/or N5991PM4A releases.

Table 4. PCIe U.2 & M.2 spec test options

Transfer rate	N5991PU4A	N5991PM4A
8 GT/s	M8040A or M8020A -16G/-8G [1]	M8040A or M8020A -16G/8G [1]

1. M8020A-16G is an M8041A module with option -C16
M8020A-8G is an M8041A module with option -C08

PCI Express receiver test product add-ons

Different add-on licenses are available for the N5991PxxA PCI Express RX test automation product family. An add-on gives its capabilities to all test automation licenses of the family it belongs to.

N5991PA1A-ADD PCI Express integrated BER counter interface support

Support of the DUT-integrated BER-counter interface is added by the N5991PA1A-ADD add-on.

N5991PA2A-ADD PCI Express multi-channel support

Support for multi-channel testing is provided by the N5991PA2A-ADD add-on. This add-on allows you to configure more than two channels. It requires a multi-channel M8000 BERT system with more than two channels. Currently this is possible with M8020A systems up to 16 GT/s only. Up to two channels can be configured without the N5991PA2A-ADD option. Tests or calibrations are performed sequentially and not in parallel.

N5991PA3A-ADD PCI Express link EQ test support

Link equalization RX tests as well as link equalization TX require the N5991A3A-ADD add-on.

N5991PA4A-ADD PCI Express receiver test switch system support

Support for BitifEye switch matrixes can be added by the N5991A4A-ADD add-on. Supported are BitifEye's BIT-2100B switch system x4, x6 and x8 configurations. For 2.5 GT/s, 5 GT/s and 8 GT/s it is possible to calibrate each lane individually. For 16 GT/s only lane 0 is calibrated and the user must ensure that all other lanes have similar characteristics since the lane 0 calibration is applied to all other lanes. Switch matrixes are not supported for 32 GT/s or higher. The multi-channel add-on N5991PA2A-ADD is not required.

More information on the add-ons can be found in the N5991A data sheet.

PCI Express link training suite

The PCIe link training suite simplifies the process of creating static training sequences. Next to a graphical representation of the loopback path through configuration and the required parameters, the PCIe link training suite software tools offer a scripting language which is helpful for the creation of more specialized sequences. N5991PL5A supports transfer rates from 2.5 GT/s to 32 GT/s, while N5991PL4A supports transfer rates up to 16 GT/s. Both products support the M8020A BERT system, as well as the M8040A BERT system.

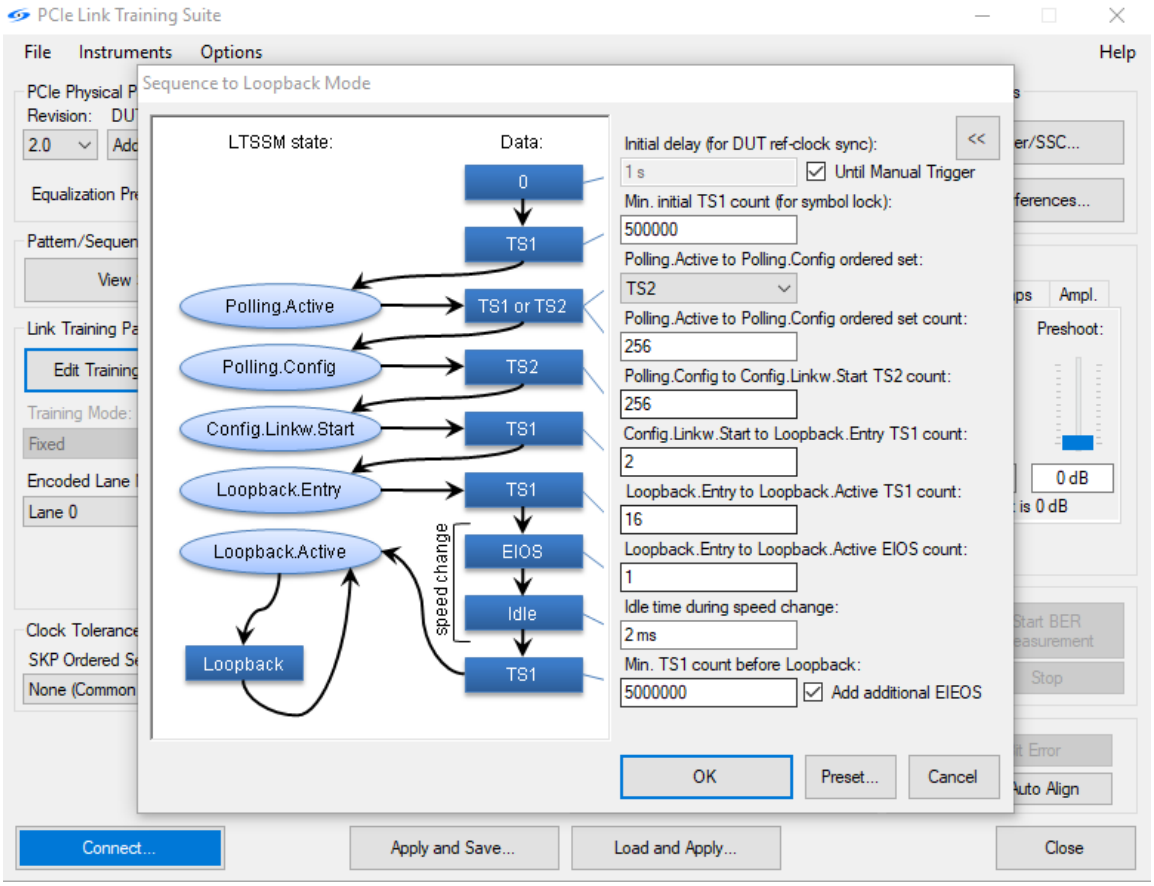


Figure 18. Generate static training sequences for PCI Express using the PCIe link training suite

Protocol Layer Test

PCIe protocol test challenges are increasing

A single PCIe interface may be part of a component which uses higher layer protocols that leverage PCIe, such as Non-Volatile Memory Express® (NVMe®) for storage applications, or the emerging Compute Express Link® (CXL®) specification for attaching accelerators and sharing memory resources. Those protocols depend on a fully validated PCIe layer that is functioning properly.

With the proliferation of PCIe use cases and applications, the need for reliable PCIe protocol debug tools that can be deployed quickly and trusted has become critical for validation labs.

The challenges are not limited to the higher layer protocols, although those are complicated. The PCIe 6.0 speed step to 64 GT/s makes link training and speed negotiation even more difficult than previous generations. During integration of PCIe transceivers into product, engineers pay close attention to proper equalization and training settings. Protocol tools that can provide validation engineers with an exact view of the operation of the Link Training Sequence State Machine (LTSSM) are necessary.

Some of the most troubling PCIe issues occur during the bring-up sequence, where link partners fail to negotiate to the highest mutually supported speed, links have high bit error rates, or links operate in degraded modes, or frequently restart. Having a protocol analysis tool that provides a clear and accurate view of how the protocol and LTSSM are working is important.

In designing the Keysight PCIe 6.0 and 5.0 protocol solutions, engineers prioritized signal integrity, recognizing that trustworthy electrical performance is the foundation for a reliable protocol analysis strategy.

With this focus, Keysight protocol test solutions for both PCIe and CXL were developed. Keysight protocol analyzers come in three classes. The LA1-class includes the logic analyzers, while the LA4-class includes the DDR logic analyzers. The LA5-class includes the PCIe protocol analyzers, exercisers, and backplanes.

The foundation for accurate protocol analysis: reliable signal integrity

Debugging complicated interoperability issues between a PCIe host and device requires that any protocol analyzer interposer does not disrupt the interactions between the two. The foundation of this in Keysight's PCIe 6.0 and 5.0 protocol solutions is superb control of signal integrity with built-in equalization and amplification that can effectively remove the effects of the analyzer from the link. This provides the user with confidence that the traffic observed between the host system and endpoint is exactly as if the analyzer were not present.

Other analyzer designs that rely on a separate analyzer chassis often introduce physical and electrical complexities that can impact the channel. In some cases, these interposers inadvertently add channel impairments which can affect the system under test such that it cannot reliably negotiate to the highest mutually supported speeds and lane width. In other cases, an interposer may introduce retiming or redriving capability that can mask issues in the system under test by effectively improving the channel quality and enabling devices to successfully link up in configurations that could not be attainable without the analyzer present. Neither of these conditions is acceptable as they impede the ability of the test and validation engineer to gain a clear and accurate view of what is happening on the link.

The P5570A PCIe 6.0 and the P5552A PCIe 5.0 protocol analysis solutions were designed deliberately to avoid these issues, to minimize channel impact and to provide the clearest and most accurate view of the traffic on the PCIe link. Thus, test and validation engineers can focus time and energy on solving protocol issues between the products under test, rather than questioning whether issues have been introduced or masked by their test equipment.



Figure 19. The P5570A PCIe 6.0 protocol analyzer

The Keysight PCIe protocol analyzers enable deep protocol analysis of PCIe systems in a form factor that is easy to deploy on the lab bench and offer unparalleled signal integrity. The P5570A / P5552A analyzers support capture and decoding for PCIe 1.0 through PCIe 6.0 / 5.0. By removing the need for a cumbersome external analyzer chassis, setup and versatility on the lab bench are greatly improved. Additionally, this simplified design yields superior signal integrity, ensuring that the analyzers have minimal impact on the channel between the products under test.

The P5570A / P5552A analyzers enable decoding of up to 64 GT/s / 32 GT/s signaling and lane widths of x 4, x 6 and x 16. Users can utilize up to 16 GB trace depth memory aided by on-board compression which greatly expands the available capture time. The analyzers support decoding of the physical layer (TS1 / TS2 / ordered sets), link layer (ACK / NAK, sequencing numbers, replay, etc.), and transaction layer (memory, config, and I/O read and write operations, etc.).

The P5573A PCIe 6.0 and the P5551A PCIe 5.0 protocol exercisers allow test engineers to emulate both PCIe root complex and endpoint devices when validating PCIe designs. The exercisers support traffic generation from 2.5 GT/s through 64 GT/s / 32 GT/s/ and lane widths from x 1 to x 16. They include over 100 built-in LTSSM test cases, error insertion capability at the transaction layer and the data link layer, and a protocol checker.

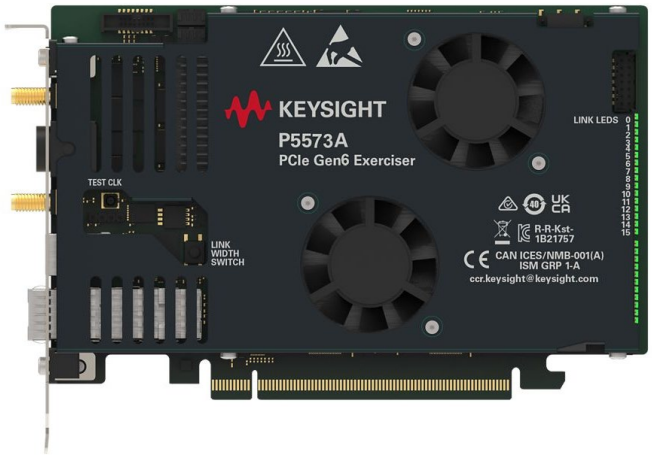


Figure 20. The P5573A PCIe 6.0 protocol exerciser

The P5573A and the P5551A use an integrated, single add-in-card design which greatly simplifies the connection and setup of the tool while offering greatly improved signal integrity compared to other architectures. This enables test and validation engineers to focus their time and energy on designing and automating unique test cases for their products, rather than wasting time dealing with an overly complex test setup with poor signal integrity.

Backplane test platform



Figure 21. The stable mechanical construction of the P5563A PCIe 6.0 protocol backplane enables reliable operation during bring up.

The Keysight P5563A PCIe 6.0 protocol backplane test platform features signal integrity enhancements to reduce crosstalk and improve signal integrity, where low-loss material in utilized to support reliable connections from 2.5 GT/s up to 64 GT/s.

Convenient and stable mechanics

The single-card design of the Keysight protocol analyzers enables a convenient and fast setup on the lab bench. Often test configurations on the lab bench quickly become complicated and instable. Mechanical stability of prototype devices is critical though to ensure that early product samples are physically protected and that the mechanical connection between the analyzer and the product under test is solid and robust to avoid any signal impairments introduced by mechanical instability. The P5552A and the P5570A are provided with a bracket mount that enables secure attachment within many server chasses. Additionally, attention has been given to providing mechanical security to add-in-card endpoints that are included in the test setup via an additional stability bracket.



Figure 22. The P5570A PCIe 6.0 and the P5552A PCIe 5.0 protocol analyzers' new form factor integrates both the analyzer and interposer into one integrated design, simplifying connections.

Above the standard PCIe server mounting bracket, an additional mount point is provided to attach the Keysight P5500A card holder. This card holder ensures a secure mechanical connection between an add-in-card and the P5570A or P5552A analyzer. Further, it provides physical protection to the add-in card. Often, products under test on the lab bench are part of limited prototype runs, and the loss of a single unit to poor mechanical stability is a real risk to product validation timelines. The Keysight protocol analyzers enable test and validation engineers to mitigate those risks. This eliminates doubts from the validation process and ensures that engineers are not chasing problems introduced by a poorly designed mechanical setup that introduces electrical and protocol errors due to instability.

Combined PCIe exerciser and analyzer software

Keysight PCIe protocol exerciser and PCIe analyzer can be driven by a single combined software interface, offering the user easy access to all the powerful capabilities of both tools. Through a simple tab-based interface, the user can configure the exerciser and analyze r side by side with just a few clicks. The P5577PSWA PCIe 6.0 and the P5551PSWA PCIe 5.0 protocol exerciser GUI provide deep functionality for configuring traffic setup, while also providing improved data exchange with the analyzer.

Via this thoughtfully designed interface, the user can configure all the most important characteristics of the PCIe link such as lane width and link speed.

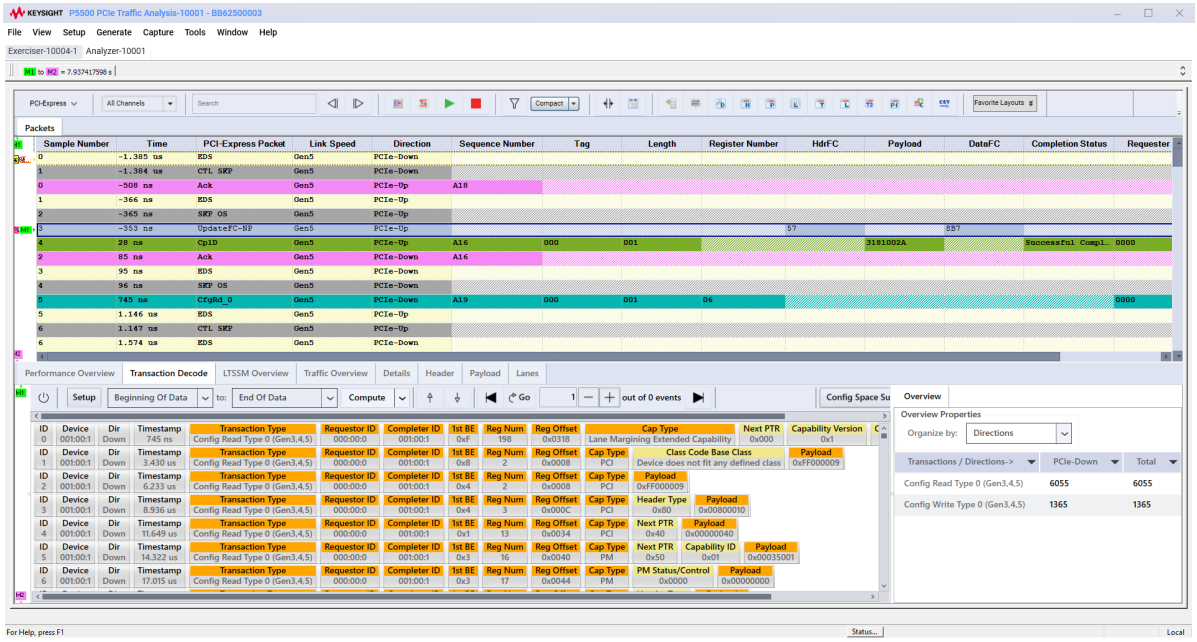


Figure 23. PCIe protocol analysis: TLP trace

Powerful triggering and filtering

The most difficult bugs to solve are intermittent with no obvious cause. Finding the root of these troublesome issues often involves setting up for long capture times. But capturing lots of data is not helpful if it cannot effectively be analyzed. Scrolling through trace captures looking for specific issues that are obscured by retraining events and other protocol ‘storms’ is an ineffective use of time.

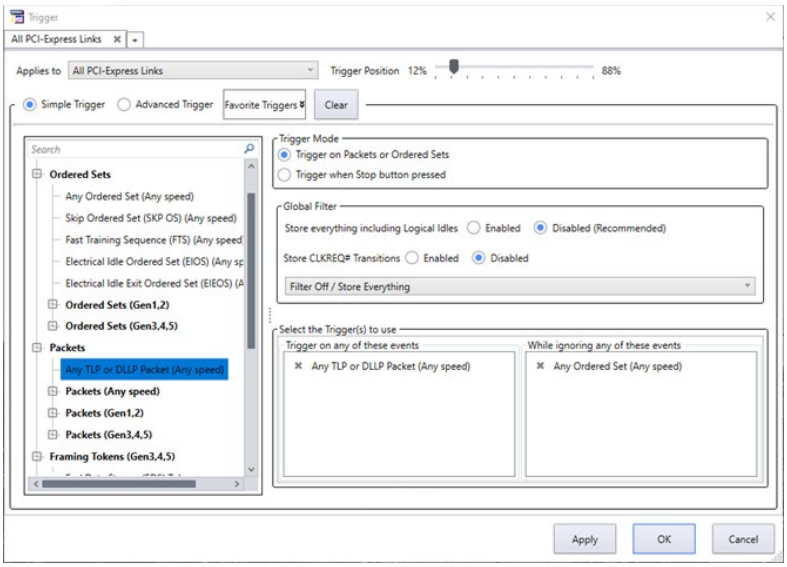


Figure 24. Various trigger and filter settings are available to enable capturing of specific protocol events

Advanced users depend on finely tuned triggering and filtering settings to capture the traffic that they are most interested in. They avoid massive capture windows that scoop up unwanted data which slows down the analysis process both in porting the data to a PC for viewing as well as needlessly obscuring critical protocol events. The Keysight protocol analyzers were designed with this use case in mind. As such, they provide both simple and advanced triggering modes. Simple triggers are provided that are quick for users to apply and customize. Advanced triggers can be configured to apply a chain of if/then logic steps to the trigger. In this way specific protocol events can be captured easily, even if they occur only after a complex series of previous events that may span a long period.

To extend this capability, even further filtering can be applied to ignore certain traffic events to extend the capture window without clogging up the capture log with unneeded data.

Traffic decode and analysis capability

Solving protocol issues involves a variety of skill sets and debugging tools. Some issues require being able to see specific fields in a packet. Other problems require having an overall view of traffic patterns and errors in a given time frame. To support these needs, the P5576PSWA PCIe 6.0 and the P5552PSWA PCIe 5.0 protocol analyzer software provide several different protocol views to enable engineers to use the tool most suited to the problems they are working on.

Lane view

Lane view provides the user with a view of exactly what data is appearing on which lane of the PCIe link. In a single, simple view, the user is given a comprehensive understanding of the protocol makeup.

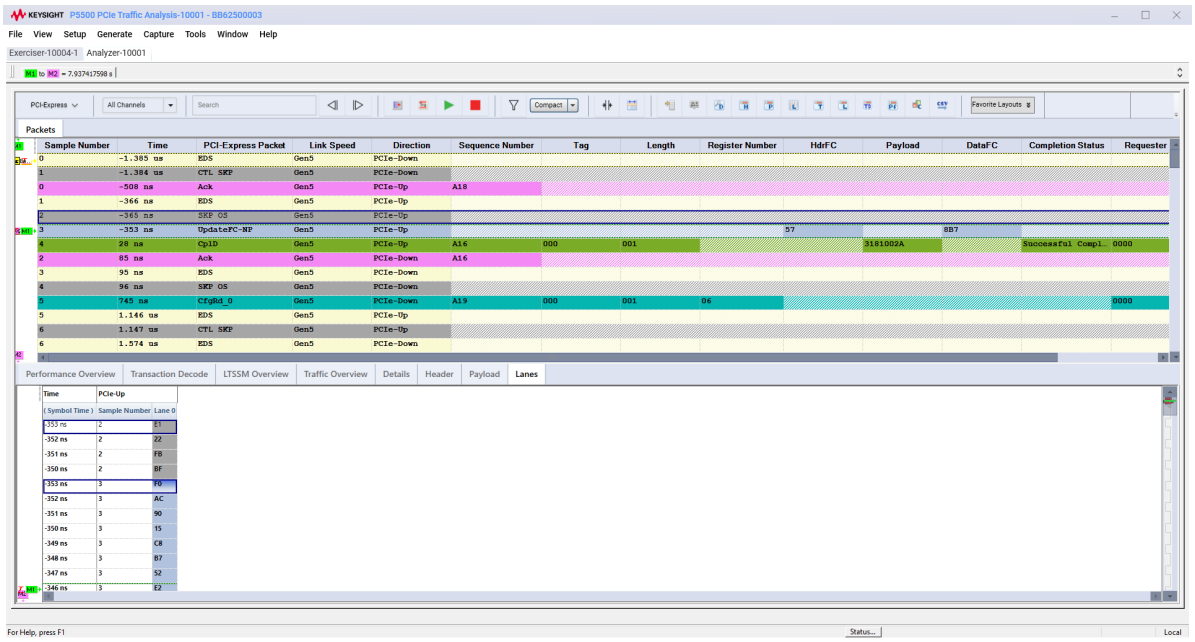


Figure 25. Lane view

Performance overview

The performance overview tab provides a visual depiction of different PCIe protocol events over time.

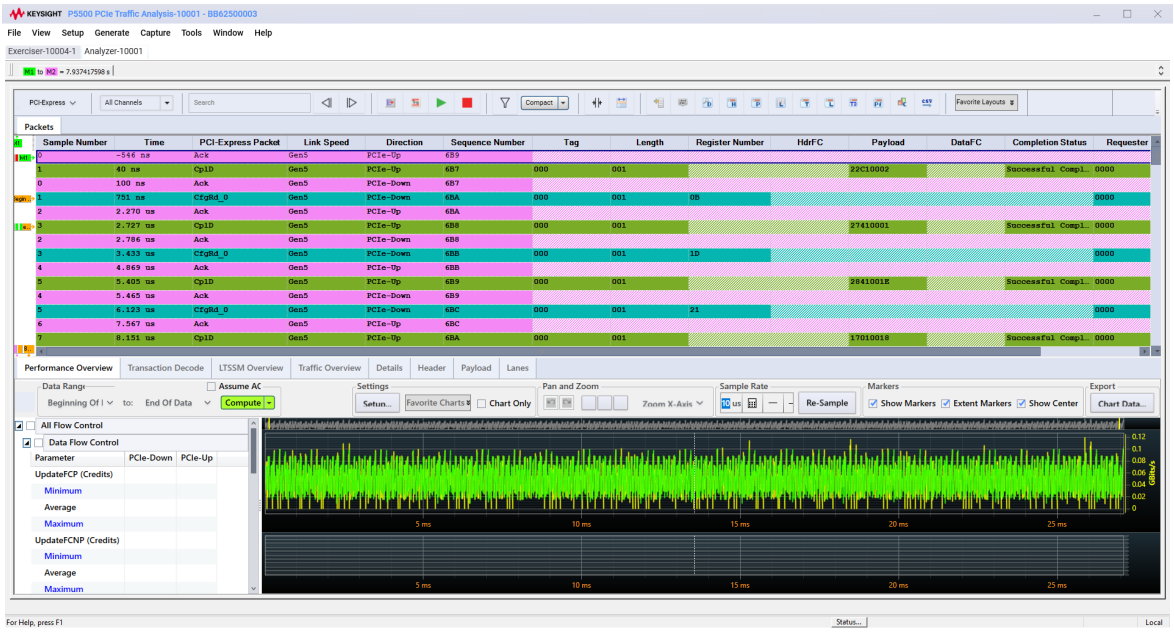


Figure 26. Performance overview

Transaction decode view

The transaction decode tab provides a detailed view of how individual packets are organized into a transaction. This provides an intuitive look at how packets are organized in the protocol.

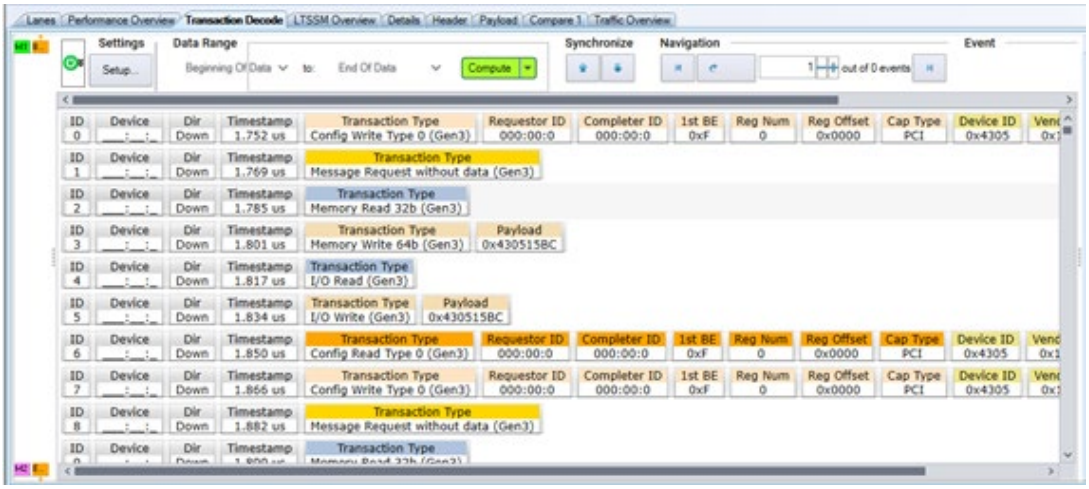


Figure 27. Transaction decode view

LTSSM overview

Proper link training is critical to solid PCIe performance, and it is often the source of many issues. Physical differences in channels and products are manifested at the protocol layer via the LTSSM. The LTSSM overview tab allows validation engineers to see progression through the LTSSM at the ordered set level, and a decode of which states both the upstream and downstream ports are in at a given moment. The LTSSM overview tab is a powerful tool for debugging one of the most difficult and complex aspects of PCIe protocol.

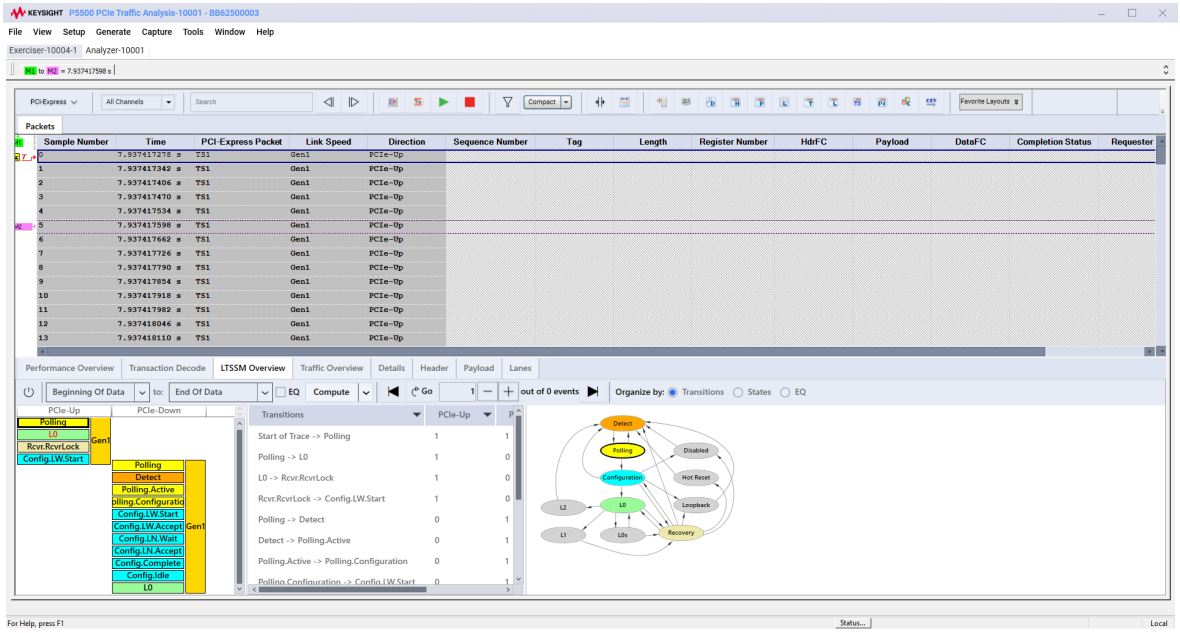


Figure 28. LTSSM overview

Get a quote on the Keysight PCIe 5.0 protocol test solution or the PCIe 6.0 protocol test solution

Use cases:

Use case - Analyze traffic between root complex and endpoint

A common use case for the Keysight PCIe analyzers is to sit between a PCIe capable root complex and a PCIe endpoint. The analyzer will capture and decode PCIe signals between the root complex and the endpoint while also passing the signals between the devices through without interference.

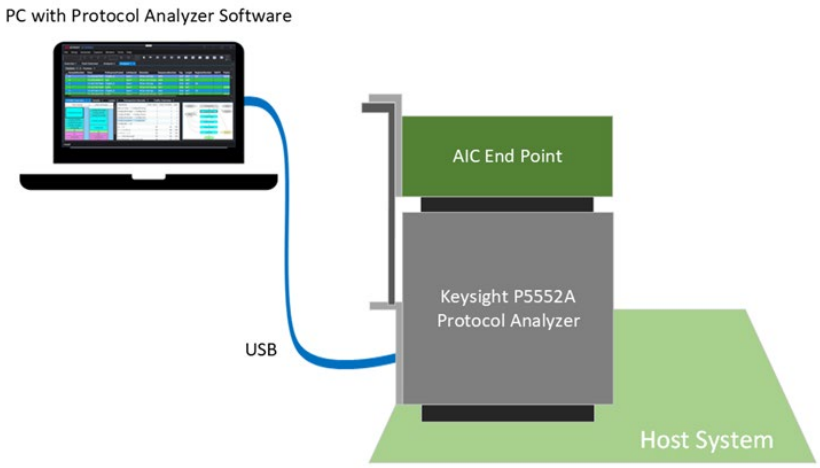


Figure 29. The Keysight protocol analyzers use an independent power supply, and pass power supplied from the host system on to the endpoint without interference.

Use case - Root complex emulation for testing endpoints

When emulating a root complex, the P5551A RAS cards can connect to a PCIe slot on the P5563A test backplane board with the end point (DUT) sitting in another PCIe slot. The exerciser then provides downstream stimulus to the DUT as a root complex just as a regular host system would. Then the exerciser can check the data received from the DUT for errors. This common configuration is simple to set up and easy for the end user to operate and troubleshoot.

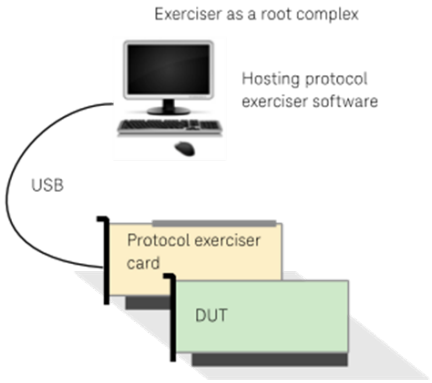


Figure 30. The Keysight P5551A can be configured to emulate a PCIe root complex with its own link, equalization, and power management parameters.

Use case – PCIe end point emulation for testing root complex

When emulating an end point, the PCIe exerciser card can be plugged into any PCIe slot on a system motherboard, like any other PCIe add-in-card device, such as a network interface card (NIC), graphics card, or solid-state drive (SSD), would be plugged in. Multiple exercisers can be plugged into the system under test to create more complicated test setups.

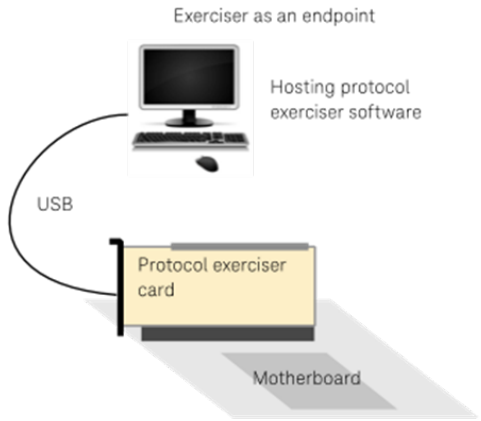


Figure 31. The PCIe protocol exerciser can be used to emulate a PCIe endpoint.

Combined CXL 1.1 and 2.0 protocol exerciser and analyzer software

The **CXL protocol exerciser** solution consists of both hardware and software. The P5561CXLA CXL 1.1 / 2.0 exerciser software is used with the P5573A protocol exerciser hardware for an integrated, CEM add-in-card design which greatly simplifies the connection to the CXL device.

The CXL protocol exerciser software supports protocol traffic generation for all CXL 1.1 and 2.0 supported speeds and lane widths from x1 to x16. The CXL exerciser can emulate a root port or endpoint, generate FLIT traffic and includes built-in LTSSM test cases, error insertion, and a protocol checker. The P5561CXLA software is used with the protocol exerciser hardware, which is designed to be easy to setup, connect, and quickly configured to bring up the CXL link and check LTSSM and protocol functionality.

The **CXL protocol analyzer** solution also consists of both hardware and software. The P5562CXLA CXL 1.1 / 2.0 analysis software is used with the P5570A protocol analyzer hardware and offers a cableless CEM form factor for a robust and reliable setup that is easy to deploy on the lab bench and offers unparalleled signal integrity.

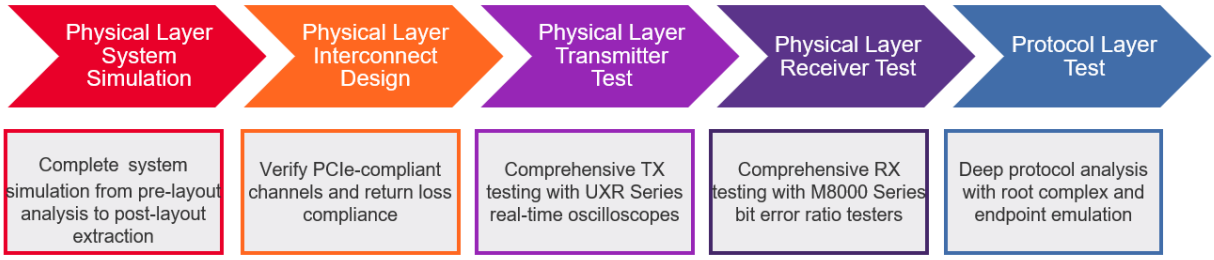
The CXL protocol analyzer software enables comprehensive analysis and visualization capabilities for CXL.io, CXL.mem, and CXL.cache. The protocol analyzer sits between the root port and endpoint to capture and decode the transactions on the CXL bus. The P5562CXLA software is used with the protocol analyzer hardware which integrates the interposer and analyzer into a unique CEM card form factor that simplifies connection to the device and offers unparalleled signal integrity.

Summary

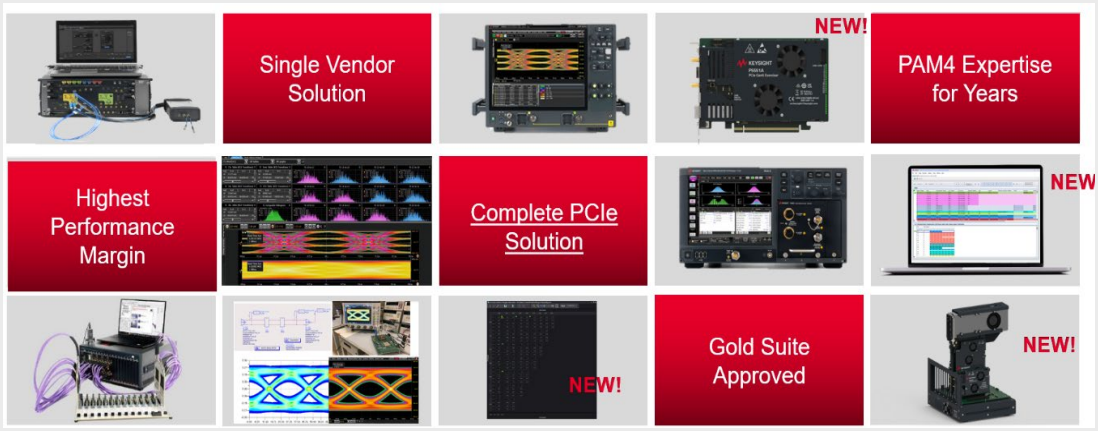
PCIe 6.0 products are now reaching the market. While maintaining backwards compatibility to previous generations, the PCIe 6.0 interface doubles the transfer rate to 64 GT/s, providing throughput of 256 Gb/s over the same maximum of 16 lanes. One way this is accomplished is by adopting PAM4 signaling for PCIe, which doubles the data encoded in each transition. The introduction of this new encoding scheme adds a layer of complexity which will require robust test solutions. Regardless of which generation of the PCIe specification you are working on, you need a test solution approved by PCI-SIG to ensure that your products comply with the standard and get to the market faster. Keysight provides a total-solution approach to test all generations of the PCIe specification, so you can focus on your next design, rather than spending time learning the details of the test procedures and requirements.

You need a smooth transition from PCI Express® 5.0 to 6.0 where the integrity of your PCIe measurements is backed by standards knowledge and leading-edge tools. PCI Express 6.0 is a challenging technological leap especially with the move from NRZ to PAM4 and eye heights of only 6 mV.

Keysight helps define the future of PCI Express as a representative on the PCI-SIG Board of Directors and a major participant in working groups. We provide the most complete and scalable PCIe testing solution showing the true performance of your design, improving your time to market and streamlining your path to PCIe success.



Your pathway to PCIe 6.0 success



For more information

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Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.

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