WHITE PAPER



Reducing High-Speed Digital Validation Bottlenecks Through Efficient Workflows

KEYSIGHT

The Rising Complexity of High-Speed Digital Validation

High-speed digital validation has become one of the most demanding tasks in modern product development. Whether developing PHY silicon or designing embedded interfaces, today's developers must validate interoperability across a growing set of high-speed protocols.

Many digital standards, like USB4 Version 2.0 (USB4v2), LPDDR6, and PCIe 6.0, are getting more complex and time-consuming to validate. Each generation brings higher data rates, higher levels of modulation, and tighter performance thresholds.

Compliance testing ensures products communicate reliably to the standard, but it can become a major development bottleneck. Both validation and compliance test cycles can stretch for weeks, forcing redesigns and pushing out schedules. As signal speeds accelerate and compliance thresholds shrink, developers must test faster, characterize signal behavior more accurately, and work more efficiently to keep pace with innovation.

This paper examines the industry trends driving increasing cycle times and test complexity, explores the biggest bottlenecks facing developers and validation engineers, and shares practical strategies for accelerating validation while improving confidence in interoperability and performance.

Industry Trends Driving Validation Bottlenecks

AI data centers and high-performance computing continue to push interface standards to new extremes. Meanwhile, consumer and embedded devices are quick to adopt the same technologies. As a result, three common trends are affecting engineers responsible for validation and compliance.

- **Compressed development cycles:** The demand for throughput and capacity is accelerating new standards and shortening development timelines (Figure 1). Developers must ramp up on new standards and deliver compliant designs faster than ever.
- **Shrinking margins:** New standards introduce multilevel modulation (PAM3 / PAM4), tighter jitter / signal-to-noise-and-distortion ratio (SNDR) thresholds, and more equalization presets. Advances in process nodes enable higher speeds but reduce tolerance for error. Even minor signal integrity issues, like crosstalk, return loss, or intersymbol interference, can trigger a compliance failure or system instability.
- **Lab constraints:** Validating these interfaces requires high-bandwidth oscilloscopes, bit error rate testers (BERTs), and arbitrary waveform generators (AWGs). These instruments demand dedicated bench space, power, and cooling. These constraints limit collaboration, reduce mobility, and slow workflow efficiency.

Together, these issues create three bottlenecks: test time, measurement confidence, and workflow efficiency. In the following sections, we'll examine each bottleneck in depth and discuss methods to overcome them.

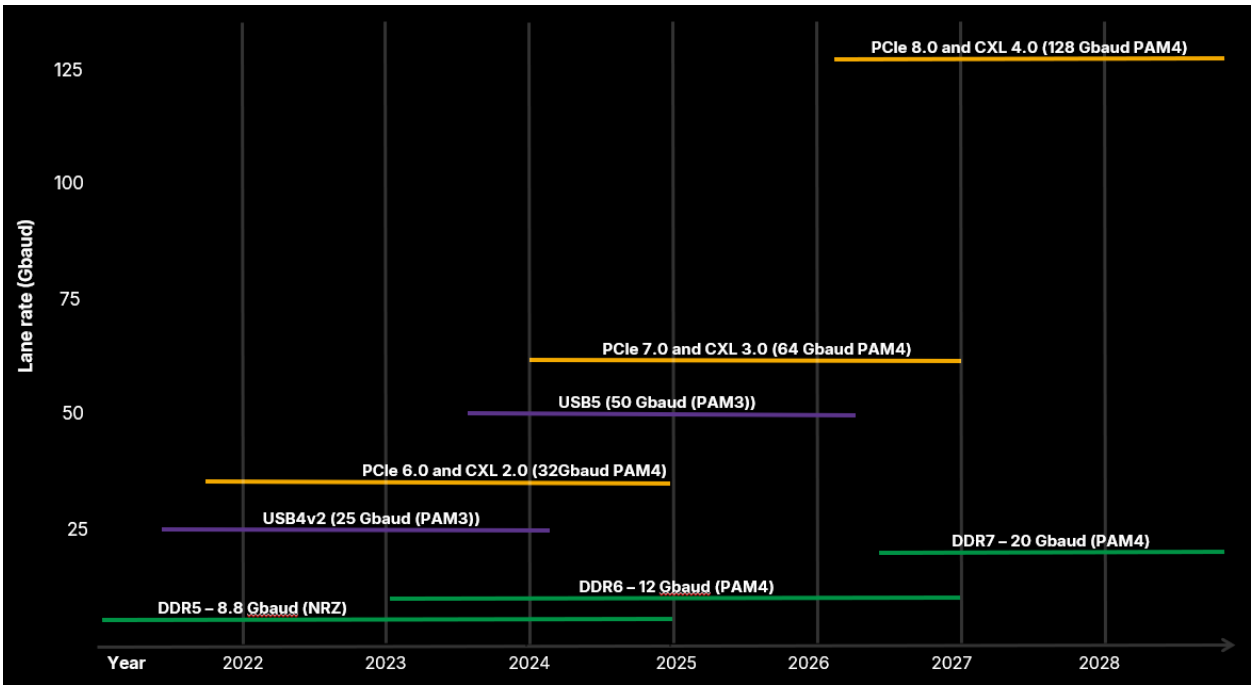


Figure 1. Standards development timelines are shrinking, with each new generation projected to arrive faster than ever, shorten development lifecycles, and double data rates.

Long Test Cycles with Shorter Deadlines

Digital validation can put release schedules at risk. Even with automation, full compliance suites can take hours — or days — because of manual steps, single-threaded analysis, and repeated testing under various conditions.

Why Validation and Compliance Cycles Take So Long

- **Manual setup and calibration:** Many test cases require configuration, cable swaps, and calibration. Each step extends cycle time and introduces opportunities for human error. Poor signal integrity in an instrument setup can give inconsistent results across multiple test cycles.
- **Exhaustive measurement requirements:** Modern standards define dozens of parameters across every lane. For USB4 and DisplayPort 2.1, this includes voltage and timing margins, rise / fall times, jitter decomposition, equalization behavior, and bit error estimation under worst-case conditions.
- **Repeated signal conditions:** Compliance tests require evaluating performance across a range of stressed conditions, including worst-case conditions, under varying data patterns, thermal conditions, and crosstalk from adjacent lanes. Each scenario adds another layer of repeated measurements.

Approaches to Reducing Long Test Cycles

Validation teams can use a few methods to mitigate time-intensive test cycles:

- **Parallel test stations:** Running multiple oscilloscopes in parallel increases throughput but not the test time per device. For that reason, this approach is used primarily in manufacturing test lines.
- **Server disaggregation:** Because signal analysis is the largest portion of a test cycle, with acquisition accounting for approximately 25%, teams can use a single oscilloscope for acquisition and offload processing to external servers. This can reduce cycle time but increases cost and complexity with additional hardware and network support.
- **Multicore processing:** Many oscilloscopes still rely on single-threaded analysis. Multicore architecture runs measurements in parallel, dramatically reducing processing time. Measurements such as jitter and rise time can drop from minutes to seconds.

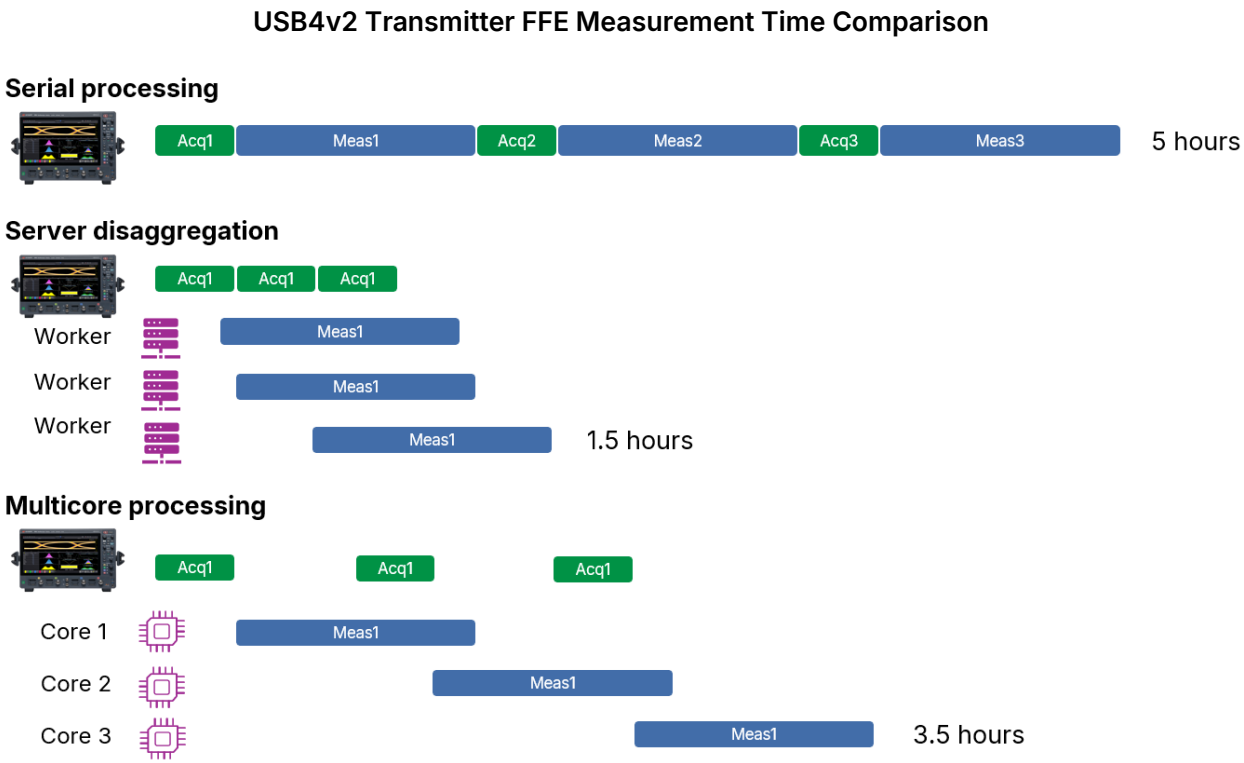


Figure 2. Test times for three different test approaches to make the USB4v2 transmitter feed forward equalization (FFE) measurement. While the multicore oscilloscope is significantly faster than the standard one, this measurement benefits most from server disaggregation.

As Figure 2 shows, each setup gives drastically different results, and this varies per measurement. By choosing a test workflow that best disaggregates signal analysis for the measurements they're making, engineers can cut compliance cycles from days to hours, reducing bottlenecks in development.

Tightened Thresholds and Shrinking Measurement Margin

As specifications tighten, designers face narrower timing and noise margins, reduced jitter tolerance, and multilevel signaling. High-fidelity measurements become both harder and more critical.

Limited measurement margin can produce misleading or ambiguous results. A marginal device may appear to pass, or a compliant device may falsely fail, due to instrument noise near the margins. Moreover, repeatability matters just as much as accuracy. Inconsistent results can slow debugging and destroy confidence in a device's compliance with specifications.

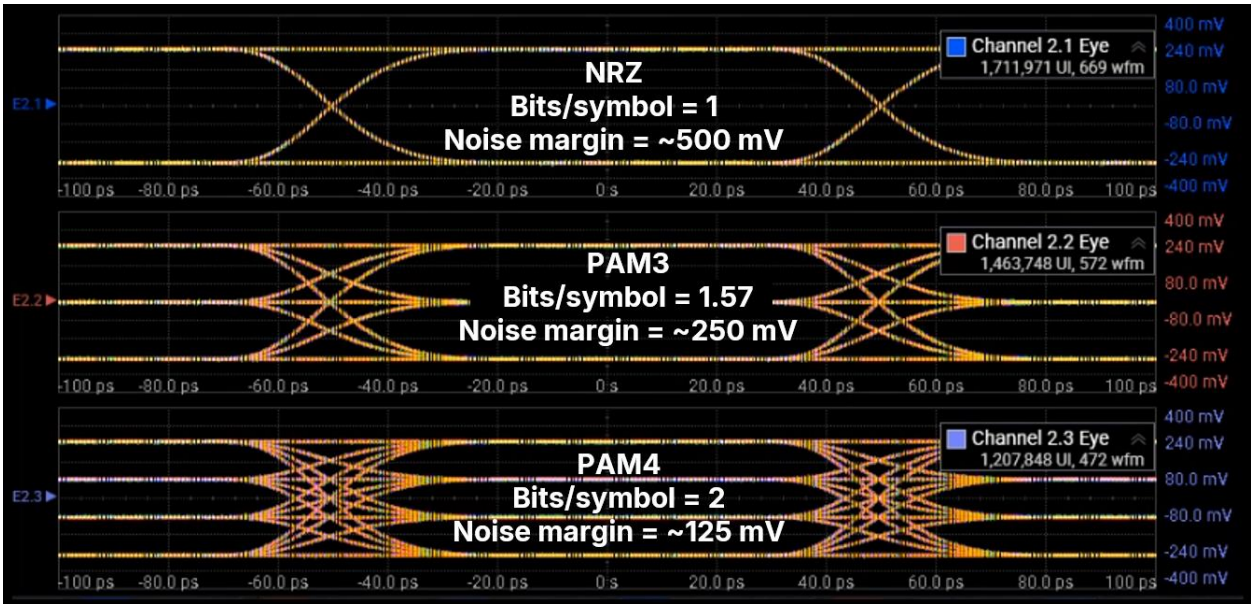


Figure 3. Reduced vertical eye height from multilevel modulation

The Drivers of Measurement Complexity

New standards requirements increase both the number of measurements needed and the fidelity required to accurately measure them.

- **Reduced vertical eye height:** Multilevel modulation compresses the voltage levels between symbol states, increasing susceptibility to vertical noise and making eye closure harder to detect (Figure 3). New specifications like SNDR have been added to standards like USB4v2 to better characterize these issues.
- **Jitter decomposition requirements:** Today's compliance tests require separating total jitter into deterministic, random, and sinusoidal components. Accurate decomposition requires high-fidelity waveform capture and precise timing measurements (Figure 4).
- **Multiple simultaneous eyes:** Multilevel signaling schemes create multiple overlapping eye diagrams. For example, PAM4 has three eyes per lane, each of which must meet independent criteria for rise / fall times, jitter, and signal-to-noise ratio.
- **Inter-lane and crosstalk effects:** Dense multilane interfaces compound complexity. Compliance tests specifications often apply to testing one lane at a time. However, interference between lanes can mask subtle errors or create false failures if the instrument cannot isolate signals cleanly.
- **Complex equalization and filtering requirements:** Standards like USB4v2 expand the number of transmitter equalization presets, each of which needs to be evaluated to ensure optimal link performance between transmitter and receiver.



Figure 4. Raw waveform, eye diagrams, and jitter decomposition measurements of two digital channels

Improving Signal Integrity for Reliable, Insightful Measurements

To address the challenges of more complex signaling, validation teams need to upgrade to improved hardware and software solutions.

1. **High-resolution analog-to-digital converters (ADCs):** Higher resolution reduces quantization noise as shown in Figure 5, exposing small signal variations, marginal eye opening, vertical noise, and subtle equalization behavior.
2. **Lower intrinsic noise:** A lower noise front end preserves waveform shape and increases measurement margin near pass / fail thresholds.
3. **Specialized analysis tools:** Compliance software can emulate equalization settings for specific standards, while signal integrity software can de-embed test fixture effects or model worst-case conditions.

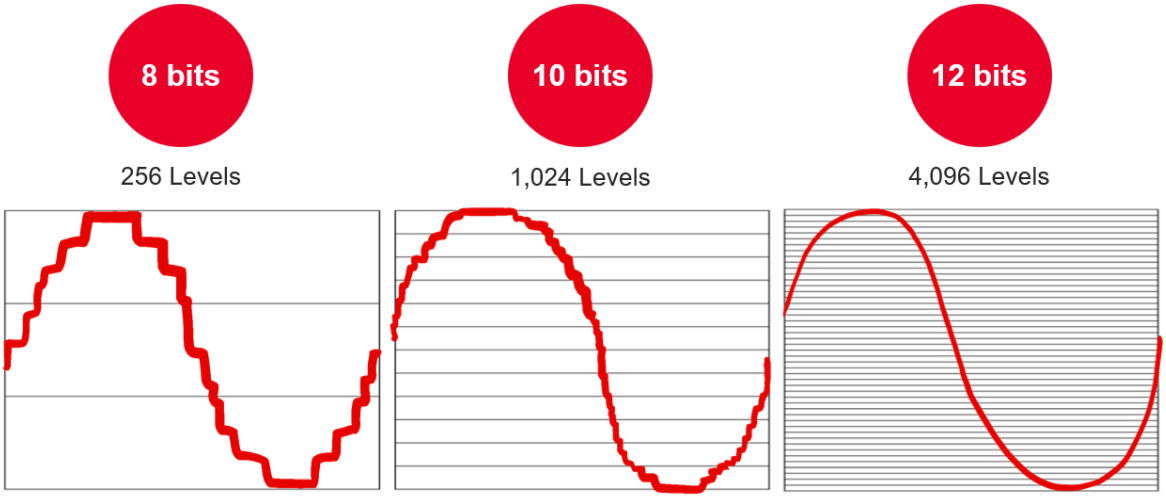


Figure 5. ADC resolution comparison showing differing levels of signal quantization

With higher-fidelity acquisition and strong measurement analysis software, teams can gain more trustworthy, actionable insights. Higher resolution and lower intrinsic noise improve the effective number of bits (ENOB), an overlooked measure of an instrument's signal integrity. High ENOB strengthens confidence in compliance results and accelerates debugging.

Lab Constraints That Limit Validation Workflows

High-performance oscilloscopes, BERTs, and AWGs are essential for validation, but they create workflow constraints. Validation setups require significant bench space, dedicated power, and airflow considerations.

The weight and size of the instruments make them difficult to move. Cooling fans required to prevent overheating can be extremely loud, making collaborative use uncomfortable.

These may seem like minor inconveniences, but over time, they can force teams to work around the instrument rather than focusing on analysis and problem solving.

Rethinking Instrument Design for Modern Validation Workflows

Fixing thermal management will help alleviate constraints. Modern oscilloscopes are high-performance computers attached to sophisticated front-end acquisition paths. They run at high sample rates and require substantial compute power, generating significant heat. To maintain consistent performance over long test runs, traditional oscilloscopes rely on large heatsinks and fans to transfer heat, adding weight, size, and operating noise.

Thermal management improvements can come from both mechanical design and software efficiency.

- **Software designed for parallelism:** More efficient software design not only decreases cycle times; it can have major effects on hardware design as well. Leveraging multiple processor cores to distribute workloads, an oscilloscope can perform complex analysis with less power draw. More efficient operation lessens the need for oversized cooling systems.
- **Improved thermal architecture:** Better airflow, optimized exhaust paths, and efficient internal component layouts reduce heat buildup, which can affect measurement reliability (Figure 6). Smaller, lighter instruments have more stable operation.

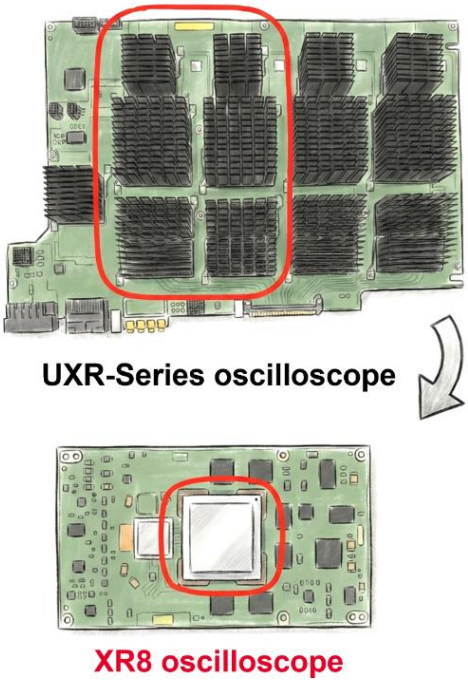


Figure 6. By integrating the ADC, DSP, memory controller, and buffering functions on a single chip, the Keysight XR8 oscilloscope has a smaller footprint and more power-efficient design compared to a Keysight UXR-Series oscilloscope

The result is a faster, more reliable oscilloscope that fits better into modern labs. Lower power draw allows operation from standard outlets, while a smaller footprint frees up bench space for fixtures and other equipment. A lighter chassis can be more easily transferred between labs, and quieter operation creates a more comfortable, collaborative environment for validation teams.

With these constraints removed, engineering teams can evolve their workflows, focusing on problem solving, not equipment management.

How Validation Teams Can Stay on Schedule

High-speed digital interfaces are evolving faster than validation workflows. To stay on schedule, teams increasingly need parallel processing, accurate and repeatable signal acquisition, and instruments that fit modern validation lab workflow needs.

Teams looking to cut compliance test time and sharpen insights can explore modern, lab-friendly instruments like the Keysight XR8 oscilloscope (Figure 7). The XR8's multicore software architecture accelerates signal acquisition and analysis, providing instant insights into complex signal behavior with up to 33 GHz. The 12-bit, low-noise front end captures microvolt-level anomalies and picosecond jitter that other scopes can miss. Compact, quiet, and energy efficient, the XR8 fits comfortably into any lab, reducing setup constraints and enabling flexible workflows.

For validating and ensuring compliance at even higher bandwidths, teams should consider the Keysight UXR-Series oscilloscope, with up to 110 GHz bandwidth and compliance software that support today's standards and enable research into the next generation.



Figure 7. Keysight XR8 oscilloscope with multicore processing, 12-bit ADC, and lower power consumption and footprint than similarly-rated oscilloscopes.

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